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Controller for compensation of unbalance and harmonic distortion in an UPS inverter

Tesis que presenta

Andrés Alejando Valdez Fernández

Para obtener el grado de

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En la opción de

Control y Sistemas Dinámicos

Director de la Tesis:

Dr. Gerardo Escobar Valderrama

San Luis Potosí, S.L.P., Agosto de 2005.

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Andrés Alejandro Valdez Fernández

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División de
Matemáticas Aplicadas y Sistemas Computacionales

Maestría en Ciencias Aplicadas con opción en Control y Sistemas Dinámicos

CONTROLLER FOR COMPENSATION OF UNBALANCE AND HARMONIC DISTORTION IN AN UPS INVERTER

Ing. Andrés Alejandro Valdez Fernández

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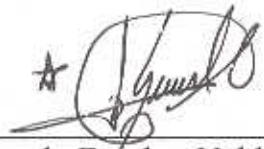

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to my parents and my sisters with gratefulness...

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RESUMEN

En este trabajo se propone un controlador basado en técnicas de control adaptable para una fuente ininterrumpida de voltaje (UPS). El controlador propuesto está basado en la medida de una corriente combinada usando un mismo sensor tipo dona para tal efecto. Esta última se forma a partir de una combinación lineal de las corrientes de capacitor y carga. El propósito de utilizar esta corriente combinada es, por una parte, obtener un comportamiento muy similar al obtenido con un controlador basado en la corriente de capacitor y por otra parte, poder obtener fácilmente un estimado de la corriente de inductor para propósitos de seguridad.

El controlador propuesto es capaz de compensar el desbalance y distorsión armónica en la carga a pesar de que esta sea de naturaleza no lineal. Técnicas de control adaptable son utilizadas para compensar las perturbaciones en los parámetros del sistema. Gracias a una sencilla transformación, el controlador propuesto tiene una forma muy similar a la de un controlador convencional, solo que este incluye un banco de filtros resonantes, los cuales confirman el Principio del Modelo Interno. El controlador propuesto está basado en descripciones en el dominio de la frecuencia de perturbaciones periódicas, es decir, incluye ambas componentes simétricas, llamadas secuencias positiva y negativa, de esta manera se puede trabajar bajo condiciones de desbalance. Como consecuencia, el controlador propuesto compensa un grupo seleccionado de componentes armónicos. En este trabajo se propone además, un estimador muy sencillo obtenido en términos de la corriente combinada y de la corriente desconocida de capacitor, debido a que la corriente combinada contiene informacion de la corriente de carga, el estimador propuesto responde de manera inmediata en caso de que una condición de sobre corriente se presente en la carga.

Por otra parte, en este trabajo de tesis, se explica con detalle la construcción de un prototipo UPS trifásico de tres hilos que soporta una potencia de 1.5 KVA, el cual fue construido para probar de manera práctica el controlador y el estimador propuestos. En este prototipo se consideran todas las precauciones necesarias, tales como, corto circuito, bajo voltaje, sobre voltaje, aislamiento galvánico entre la etapa de potencia y la etapa de control, etc. En esta implementacion tanto el controlador como el estimador propuestos son implementados por medio de una tarjeta de control dSPACE modelo 1103. Finalmente, se muestran algunos resultados experimentales representativos del desempeño del algoritmo de control propuesto en el prototipo UPS.

SUMMARY

In this thesis the control of an uninterruptible power supply (UPS) is investigated using a combined measurement of capacitor and load currents in the same current sensor arrangement. The purpose of this combined measurement is, reaching a similar performance as that obtained in a capacitor current based controller, and obtain an estimate of the inductor current for security purposes.

A controller based on the combined current measurement is proposed to compensate for unbalance and harmonic distortion on the load. Adaptation is included to cope with uncertainties in the parameters of the system. It is shown that after transformations, the proposed controller gets a simple and practical form that includes a bank of resonant filters which is in agreement with the internal model principle. The controller is based on a frequency domain description of the periodic disturbances, which include both symmetric components, namely, the negative and positive sequence, thus, allowing the treatment under unbalance operation as well. As a consequence, the controller compensates only for a selected group of harmonic components. A simple estimator for the inductor current used for protection purposes only is also proposed. The inductor current estimate is obtained in terms of the combined and the capacitor currents. Since the combined current depends directly on the current load, the estimator responds very fast to an over current in the load.

The thesis includes the design and construction of a 1.5 KVA three-phase three-wire UPS prototype to experimentally test the proposed controller and estimator. The prototype contains all sensors and signal conditioners as well as the required protections, providing galvanic isolation between the power stage and the control stage, for a safe operation. The experimental results obtained in the prototype are presented here to assess the performance of the proposed algorithm.

CONTENTS

NOTATION

Frequent Acronyms

AC	alternating current
ADC	analog-to-digital converter
ADP	analogical digital port
BPF	band pass filter
CE	chip enable
DC	direct current
DSP	digital signal processor
IGBT	isolated gate bipolar transistor
KCL	Kirchhoff's current law
KVL	Kirchhoff's voltage law
LC	inductor-capacitor
LPF	low pass filter
LTI	linear time invariant
OPWM	optimum pulse width modulation
PWM	pulse width modulation
SPWM	sine pulse width modulation
RMS	root mean square
THD	total harmonic distortion
UPS	uninterruptible power supplies
VSI	voltage source inverter

Most common mathematical symbols

$\mathbb{R}$	field of real numbers
$\mathbb{R}^n$	linear space of ordered n-tuples in $\mathbb{R}$.

$\triangleq$	"defined as"
$(\cdot)^T$	transpose operator
$(\cdot)^{-1}$	inverse operator
t	time, $t \in \mathbb{R}_+$
$\frac{d}{dt}, \dot{(\cdot)}$	differentiation operator
$(\cdot)_k^p$,	k-th harmonic coefficients for the positive sequence representation
$(\cdot)_k^n$	k-th harmonic coefficients for the negative sequence representation
$\mathcal{J}$	the skew symmetric matrix $\begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}$
$e^{(\cdot)}$	(natural, matrix) exponential function
$e^{\mathcal{J}(\cdot)}$	the 2×2 rotation matrix $\begin{bmatrix} \cos(\cdot) & -\sin(\cdot) \\ \sin(\cdot) & \cos(\cdot) \end{bmatrix}$
$\hat{(\cdot)}$	estimate of $(\cdot)$
$\tilde{(\cdot)}$	error between a quantity and its reference $(\cdot) - (\cdot)_d$, $\hat{(\cdot)} - (\cdot)$
$(\cdot)^*$	desired external references

Frequently used variables

$\delta_i \in \{0, 1\}$	:	switching sequence $\forall\ i \in \{1, 2, 3\}$
$\nu_i \in [0, 1]$	:	duty cycle $\forall\ i \in \{1, 2, 3\}$
$u_i \in [-1, 1]$	:	control signal $\forall\ i \in \{1, 2, 3\}$
L		inductance
C		capacitance
E		voltage source
α, β		weights for i_C and i_0, resp.
i_{Li}		inductor currents, $\forall\ i \in \{1, 2, 3\}$
i_{Ci}		capacitor currents, $\forall\ i \in \{1, 2, 3\}$
i_{0i}		load current, $\forall\ i \in \{1, 2, 3\}$
i_{mi}		combined current, $\forall\ i \in \{1, 2, 3\}$
$R_1,\ R_2$		control parameters
w_0		fundamental frequency

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1. INTRODUCTION

IN recent years uninterruptible power supplies (UPS) are being used more and more to provide emergency power to critical loads such as airline computers, life-support systems in hospitals and communication systems, among others. These systems provide protection against power outages as well as voltage regulation during power line over and under voltage conditions. The UPS systems are also excellent in terms of suppressing incoming line transients and harmonic disturbances. The growing applications and demands on UPSs has pushed the designers to produce systems with stricter specifications, such as, better voltage regulation, lower total harmonic distortion (THD), lower output impedance, better transient response, operation under nonlinear/distorted unbalanced loads and robustness to parametric uncertainties. Clearly, the problem of designing an appropriate UPS control strategy to fulfill all these stricter requirements has become more challenging.

This growing importance of UPS systems has motivated a flourishing development of different control strategies found in the literature, such as: deadbeat control [1], [2], [3], [4], sliding mode control [5], [6], [7], repetitive control [8], [9], [10], adaptive control [11], [12] and many others. Although these techniques are able to ensure good results under large signal disturbance, the THD on the output voltage due to nonlinear loads can still be quite high, especially in high power applications. Perhaps one of the most appealing techniques is the deadbeat control [1], [2], [3], [4], which is a discrete time control technique able to reduce the state variable errors to zero in a finite number of sampling steps, giving a faster dynamic response for digital implementation. Extensive research has also focused on different strategies aimed to

eliminate periodic disturbances, such as repetitive-based controllers [8], [9], [10], and adaptive control [11], [12].

In the beginning, a simple output voltage feedback loop accompanied with a sine pulse width modulation (SPWM) scheme [13] was proposed as an easy solution to obtain cleaner sinusoidal output voltage. In this technique, the load voltage is compared with a reference sinusoidal voltage waveform and the difference in amplitude is used to control the modulating signal in the control circuit of the power inverter. A more advanced technique employed a programmed optimum pulse width modulation (OPWM) scheme that was based on the harmonic elimination technique [14]. These schemes have shown to perform well with linear loads. However, with nonlinear loads those pulse width modulation (PWM) based schemes do not guarantee low distortion of the load voltage. To overcome this drawback, a real-time feedback control scheme using dead-beat control was proposed later in [2]. This technique employed the capacitor voltage and its derivative in a control algorithm to calculate the duration of the ON/OFF states of the inverter switching devices. The aim of this approach is that the capacitor voltage can reach the reference voltage at the next sampling time. Although this technique has been successfully implemented in single- and three-phase applications, it has shown the following drawbacks: 1) it is complex to implement; 2) it is sensitive to parameter variations; and 3) its control algorithm requires the estimation of the load parameters. In [15], the authors proposed a new single phase UPS with a dead beat current minor loop using the inductor current, and a voltage major loop using the capacitor voltage. The authors then extended the results with the dead beat current minor loop to the three phase inverters in [1]. Subsequently, the capacitor voltage and the inductor current have been frequently used as the feedback control signals in many different control schemes, such as, adaptive control [11], [12], sliding mode control [6], [7] and others. Perhaps the main advantage of using the inductor current approach is the facility to detect any anomaly arising in the load current, for instance a short circuit. However, this current is polluted with the load current distortion, causing a defective disturbance rejection and output voltage tracking.

To overcome such disadvantages it was proposed a new approach based on the measurements of the current in the capacitor filter, instead of the inductor current.

In [16] the capacitor current is used as the feedback variable in a two-switch inverter circuit topology to achieve a sinusoidal capacitor current. An outer voltage control loop is also incorporated for to compensate for imperfections in the implementation of the current control and thus guaranteeing load voltage regulation. More recent works using the capacitor current approach [17], [18], [19], [20] have confirmed that, the performance of UPS can be considerably improved if the capacitor current is effectively controlled. This is clear from the fact that while the output voltage is typically the controlled waveform, its time derivative is proportional to the capacitor current. It has been shown as well that a capacitor current feedback topology will exhibit better dynamic stiffness (inverse to the output impedance), a key metric in UPSs performance, than that of a controller with inductor current feedback. Moreover, since the capacitor current is small and alternate in nature, it may be sensed with a small and inexpensive current transformer. Thus, it can be considered a low cost alternative that has the potential to exhibit outstanding performance. However, since neither the load current nor the inductance current are measured, this controller is unable to detect, in a relatively short period of time, any anomaly arising on the load side. For instance, if a short circuit appears the capacitor current is maintained, theoretically, at the desired reference while the inductance current will grow unlimited in a short time with the unavoidable destructive effects.

In general terms, we can say that the implementation of the proposed controllers usually involves measurements of the output voltage and either, the inductor currents [3], [11], [12], or the capacitor currents [17], [18], [20] and in some cases, they even require measurements of the load current [19] with the idea of attenuating the effect of disturbances in the load. The capacitor voltage is introduced in these controllers in a second voltage loop to alleviate imperfections in the response due to parameter uncertainties and load disturbances. Therefore, based on the current signals used in the feedback control, we can distinguish two types of controllers: inductor current based and capacitor current based.

In this work a solution is proposed for the control of an UPS system to overcome such a disadvantage while preserving a good performance and guaranteeing balanced sinusoidal output voltages despite of the presence of nonlinear and unbalanced loads. This solution involves the use of a combined measurement of both load current and

capacitor current in the control loop. This combined measurement is performed in the same sensor as seen in Fig. 1.1, thus preserving the same number of current sensors as in a conventional controller. This will provide a linear combination, i.e., a weighted sum of both currents, which is then used as the feedback variable in the control loop. The current sensor CLN-50 is used for this propose. In the CLN-50 both conductors, the one conducting the capacitor current and the other conducting the load current, have been wired to obtain directly the weighted sum of both currents. Notice that, in the particular case where both weights are fixed to one, this combined current is simply the inductance current. On the other hand, assigning a zero weight to the load current leads to the capacitor current case. So a good performance can be obtained (close to the capacitor current based controller) if a smaller weight is assigned to the load current compared to the one for the capacitor current. It is shown that a simple estimator for the inductor current can now be implemented from the information contained in the combined current and the capacitor voltage measurements, plus the knowledge of the weights used. Although this estimate depends on the value of the capacitance, this signal is not used in the controller design, but its use is reserved for safety purposes, therefore the use of a nominal value for the capacitance is enough.

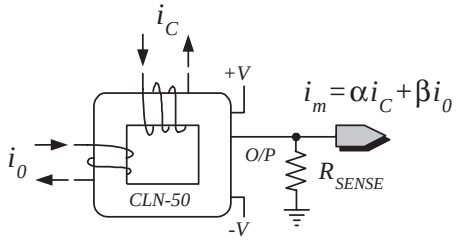

Fig. 1.1: Current sensor array to obtain the combined current.

Adaptive refinements have also been added to the proposed controller to cope with parametric uncertainties and periodic disturbances. By using the frequency domain descriptions of some unknown signals (disturbances), the solution presented here is able to perform precise voltage tracking despite of the presence of distorting loads. It reduces the effects of unbalance and harmonic distortion, likewise to other frequency domain techniques, such as repetitive control [8], [9], [10], and synchronous frame harmonic control [21]. For such purpose, the system dynamics is obtained using stationary frame quantities and the load currents (disturbance) with slowly varying

phasors. Both symmetric sequence components, positive and negative, are considered so that the unbalance operation can be treated.

In the terminology of control theory, the proposed controller performs a partial inversion of the system and adds the needed damping. The resulting system contains a disturbance term due to the uncertainty in the system parameters which is addressed via adaptation. Due to the complexity of this controller, we also propose a simple rotational transformations so that the computation complexity can be significantly reduced. Similarly to other frequency domain techniques, a group of selected harmonics are considered for compensation, and thus the proposed approach can be classified as selective since only a selected set of harmonics is targeted for compensation. The solution proposed here is based on a new, more rigorous theoretical framework, since only the disturbance terms are represented in the frequency domain and no approximations are needed for final control implementation. Finally, the proposed control scheme has been implemented and tested in a 1.5 KVA three phase inverter prototype and the experimental results are presented.

This thesis report is organized as follows. In Chapter 2, the formulation of the problem is established. In particular, the system configuration, the mathematical model, and the control objective are explained. In Chapter 3, the proposed controller is presented. In Chapter 4, all stages of the UPS system physical implementation are explained in detail. In Chapter 5, the experimental results are shown. Finally, in Chapter 6, some concluding remarks are given.

2. PROBLEM FORMULATION

2.1 System description

THE most popular setup of an UPS system is shown in its block diagram form of Fig. 2.1. The rectifier is used for converting single-phase or three-phase alternating current (AC) input into direct current (DC), which supplies power to both the voltage source inverter (VSI) and the battery bank. The VSI produces a periodical signal composed mainly of a fundamental component. The output voltage of the VSI is filtered prior to be applied to the load. An inductance-capacitor (LC) filter is typically used. This filter acts as a low pass filter (LPF) that eliminates high order harmonics leaving an almost pure sinusoidal waveform. The completed UPS system includes also stages of protection . As previously mentioned, the control signal may involve measurements of the output voltage and either, the inductor or the capacitor current measurements. Most of the material presented here has been extracted from [22] and [23].

In this work, the three-phase three-wire UPS topology shown in Fig. 2.2 is used. This is perhaps the most popular setup of a UPS system found in the power electronics literature [22]. This system includes different stages, such as, rectifier, battery bank, inverter, etc. The rectifier is used to convert single-phase or three-phase AC voltage into DC voltage, which supplies power to both the VSI and the battery bank. The VSI produces a PWM signal composed mainly of a fundamental component. The output voltage of the VSI is filtered prior to be applied to the load. An LC filter is

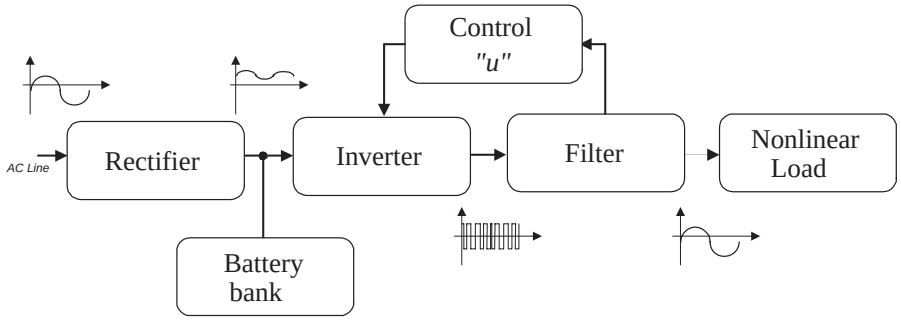

Fig. 2.1: Block diagram of an UPS system.

typically used. This filter acts as a LPF that eliminates high order harmonics due to the switching process, thus leaving an almost pure sinusoidal waveform. The overall UPS system includes also different protection circuits. As previously mentioned, the control signal may involve measurements of the output voltage and either, the inductor or the capacitor current measurements, therefore the appropriate sensors should also be provided. The control of such system is usually implemented in a digital signal processor (DSP) based board, where also the signal conditioners and operational manoeuvres to start and stop the system safely are included.

The inverter is evidently the most important part in an UPS since the good performance of the overall system will strongly depend on how well the inverter is designed and controlled. Therefore, this work concentrates on the control design for a given UPS inverter topology. There are of course different topologies for UPS, in this work the three-phase three-wire inverter shown in Fig.2.2 is studied. This topology is composed of an input voltage source, three legs (one for each phase) connected to an LC filter with the aim to generate an almost sinusoidal output voltage. Each leg consists of a cascade connection of two IGBTs, each with an antiparallel (freewheeling) diode. The IGBTs are turned on by applying a 15V signal between gate and emitter, and they are turned off with a -15V signal. The control signal applied to the gate of a given IGBT is referred as the switching sequence, which is generated in a SPWM. A drive is placed in between each SPWM and gate to reinforce the SPWM signal. Considering the Fig.2.2, the switching sequences are referred as $\delta_i \in \{0, 1\} \ \forall \ i \in \{1, 2, 3\}$. Notice that, if $\delta_i = 1$ for some $i \in \{1, 2, 3\}$ then, the respective upper IGBT is activated and if $\delta_i = 0$ for some $i \in \{1, 2, 3\}$ then, the

respective lower IGBT is activated.

2.2 Mathematical model

The modeling process starts by considering that the SPWM operates at a relatively high switching frequency. Based on this assumption, the switching sequence and the duty cycle of the SPWM can be used indistinctly in the mathematical expressions, where the duty cycle is defined as $d_i \in [0, 1]$, $\forall\ i \in \{1, 2, 3\}$. The use of the duty cycle facilitates considerably the control design since this signal is continuous, in contrast with the switching sequence that takes values in a discrete set $\delta_i \in \{0, 1\}$, $\forall\ i \in \{1, 2, 3\}$. This leads to what is referred in the power electronics literature as the average model [24]. Moreover, since most of the signals in the system have an alternate nature, it is very convenient to map the duty ratio signals towards new variables u_i, $\forall\ i \in \{1, 2, 3\}$ which take values in the range $[-1, 1]$. This is performed by means of the following transformations $u_i = 2d_i - 1\ \forall\ i \in \{1, 2, 3\}$. These new variables u_i are consider from now on as the input control signals. Let us apply the

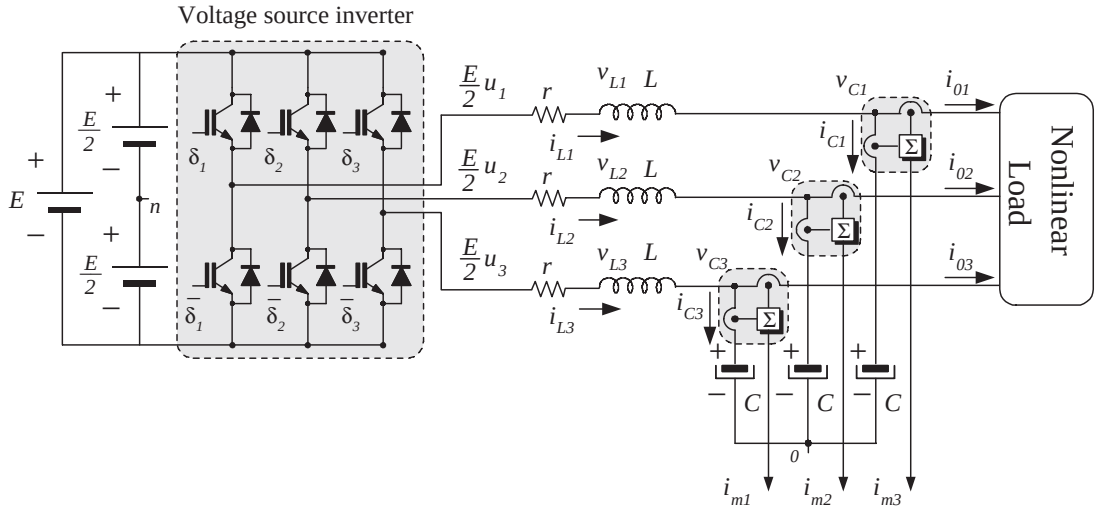

Fig. 2.2: UPS inverter system.

Kirchhoff's Voltage Law (KVL) to the electric diagram shown in Fig.2.2, taking the value of the inductors the same for each branch and assuming that they are linear

, i.e., $v_{Li} = L\frac{d}{dt}i_{Li}\ \forall\ i \in \{1,2,3\}$, and that without lost of generality the parasitic inductor resistance r can be neglect (see [25]). This yields

$$\begin{aligned} L\frac{d}{dt}i_{L1} &= -v_{C1} + v_{n0} + \frac{E}{2}u_1 \\ L\frac{d}{dt}i_{L2} &= -v_{C2} + v_{n0} + \frac{E}{2}u_2 \\ L\frac{d}{dt}i_{L3} &= -v_{C3} + v_{n0} + \frac{E}{2}u_3 \end{aligned} \tag{2.1}$$

where

L	:	inductance
C	:	capacitance
E	:	voltage source
v_{n0}	:	voltage between n and 0
v_{Ci}	:	capacitor voltages $\forall\ i \in \{1,2,3\}$
$u_i \in [-1,1]$	:	control signal $\forall\ i \in \{1,2,3\}$
α, β	:	weights for i_C and i_0, resp.
i_{Li}	:	inductor currents $\forall\ i \in \{1,2,3\}$
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i_{0i}	:	load current $\forall\ i \in \{1,2,3\}$
i_{mi}	:	combined current $\forall\ i \in \{1,2,3\}$

Table 2.1: Parameters of the UPS system.

Since three-phase three-wire topology is used, then the sum of the three inductor currents is zero. Moreover, it can also be assumed that the sum of the three capacitor voltages is zero. This permits to solve for v_{n0} from (2.1) giving the following expression

$$v_{n0} = -\frac{E}{2}\left(\frac{u_1 + u_2 + u_3}{3}\right) \tag{2.2}$$

Substituting (2.2) in (2.1) yields the following dynamical expressions

$$\begin{aligned} L\frac{d}{dt}i_{L1} &= -v_{C1} + \frac{E}{2}\left(\frac{2}{3}u_1 - \frac{1}{3}u_2 - \frac{1}{3}u_3\right) \\ L\frac{d}{dt}i_{L2} &= -v_{C2} + \frac{E}{2}\left(-\frac{1}{3}u_1 + \frac{2}{3}u_2 - \frac{1}{3}u_3\right) \\ L\frac{d}{dt}i_{L3} &= -v_{C3} + \frac{E}{2}\left(-\frac{1}{3}u_1 - \frac{1}{3}u_2 + \frac{2}{3}u_3\right) \end{aligned}$$

which can be rewritten in matrix form as

$$L\frac{d}{dt}i_{L123} = -v_{C123} + \frac{E}{2}Bu_{123} \tag{2.3}$$

where $i_{L123} = \begin{bmatrix} i_{L1}, & i_{L2}, & i_{L3} \end{bmatrix}^T$, $v_{C123} = \begin{bmatrix} v_{C1}, & v_{C2}, & v_{C3} \end{bmatrix}^T$, $u_{123} = \begin{bmatrix} u_1, & u_2, & u_3 \end{bmatrix}^T$ and the matrix B is given by

$$B = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}$$

Applying the Clarke's transformation (see Appendix A) to (2.3) yields the following model in terms of the (fixed frame) $\alpha\beta$-coordinates

$$L\frac{d}{dt}i_{L\alpha\beta} = -v_{C\alpha\beta} + \frac{E}{2}u_{\alpha\beta}, \tag{2.4}$$

where we have used the fact that $TBT^{-1} = \text{diag}\{1, 1, 0\}$.

Remark 2.2.1 Notice that the third coordinate γ has been neglected as the system considered here is a three wire topology. □

Now, applying the Kirchhoff's current law (KCL), to the system shown in Fig. 2.2, the following system is obtained

$$\begin{aligned} C\frac{d}{dt}v_{C1} &= i_{L1} - i_{01} \\ C\frac{d}{dt}v_{C2} &= i_{L2} - i_{02} \\ C\frac{d}{dt}v_{C3} &= i_{L3} - i_{03}, \end{aligned} \tag{2.5}$$

or simply

$$C\frac{d}{dt}v_{C123} = i_{L123} - i_{0123} \tag{2.6}$$

where $v_{C123} = \begin{bmatrix} v_{C1}, & v_{C2}, & v_{C3} \end{bmatrix}^T$, $i_{L123} = \begin{bmatrix} i_{L1}, & i_{L2}, & i_{L3} \end{bmatrix}^T$ and $i_{0123} = \begin{bmatrix} i_{01}, & i_{02}, & i_{03} \end{bmatrix}^T$.

After application of Clarke's transformation to (2.6), the dynamics of the capacitor voltage is expressed in terms of the fixed frame coordinates as follows

$$C\frac{d}{dt}v_{C\alpha\beta} = i_{L\alpha\beta} - i_{0\alpha\beta}, \tag{2.7}$$

Summarizing, the complete dynamics of the three-phase three-wire UPS system in the fixed reference frame, i.e., in $\alpha\beta$-coordinates, is given by expressions (2.4) and (2.7). In the rest of the thesis, the subscripts α and β are omitted to simplify the notation and to avoid confusions with the weight parameters α and β.

2.3 Control objective and main assumptions

The dynamics (2.4) and (2.7) can be rewritten in terms of i_C in the fixed frame coordinates as

$$L\frac{di_C}{dt} = -v_C + \frac{E}{2}u - L\frac{di_0}{dt} \tag{2.8}$$

$$C\frac{dv_C}{dt} = i_L - i_0 = i_C \tag{2.9}$$

$$i_m = \alpha i_C + \beta i_0, \tag{2.10}$$

where $i_L = i_C + i_0$ has been used. Notice that the combined current i_m and the capacitor voltage v_C are the only available signals.

For the controller design purposes, the following *assumptions* are considered:

A1. Parameters L, C and E are all assumed to be unknown constants.

A2. Signal u, representing the actual control, is a continuous signal proportional to the duty ratio of a SPWM switching at a relatively high frequency.

A3. Parameters α and β are the known weights that form the combined current $i_m = \alpha i_C + \beta i_0$.

A4. The current i_0 is an unbalanced periodic signal which can be expressed as the combination of a fundamental component (at a fixed frequency w_0) and its harmonics of higher order. This means that i_0 can be represented as a Fourier series of the form

$$i_0 = \sum_{k\in\mathcal{H}} \left(e^{\mathcal{J}kw_0t} I^p_{0,k} + e^{-\mathcal{J}kw_0t} I^n_{0,k}\right) \tag{2.11}$$

$$e^{\mathcal{J}w_0t} = \begin{bmatrix} \cos(w_0t) & -\sin(w_0t) \\ \sin(w_0t) & \cos(w_0t) \end{bmatrix} \quad , \quad \mathcal{J} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix},$$

where w_0 represents the fundamental frequency and vectors $I^p_{0,k}$,$I^n_{0,k} \in \mathbb{R}^2$ are the k-th harmonic coefficients for the positive and negative sequence representation, which are assumed as unknown constants (or slowly varying); $\mathcal{H} = \{1, 3, 5, 7, 11, ...\}$ is the set of multiples of the harmonic components considered. Its time derivative, used later in the control derivation, is given by

$$\frac{di_0}{dt} = \sum_{k\in\mathcal{H}} \mathcal{J}kw_0 \left(e^{\mathcal{J}kw_0t} I^p_{0,k} - e^{-\mathcal{J}kw_0t} I^n_{0,k}\right) \tag{2.12}$$

The *control objective* can now be stated as follows:

The capacitor voltages vector should be forced to track a balanced voltage reference given by

$$v^*_C = e^{\mathcal{J}w_0t} \begin{bmatrix} V_d \\ 0 \end{bmatrix} = V_d \begin{bmatrix} \cos(w_0t) \\ \sin(w_0t) \end{bmatrix}$$

which is a purely balanced sinusoidal vector signal of amplitude V_d, i.e., it is composed by a positive sequence fundamental component only. Moreover, this tracking should be guaranteed in spite of the presence of harmonic disturbances. Thus, the control objective implicitly includes two problems: the reference tracking of the fundamental component and disturbance attenuation of the output voltage to higher order harmonics produced by the distorted load current.

The equilibrium point of the overall system by forcing $v^*_C = e^{\mathcal{J}w_0t}[V_d,\, 0]^\top$ is given by

$$\bar{i}_m = \alpha\mathcal{J}w_0Cv^*_C + \beta i_0 \quad , \quad \overline{v}_C = v^*_C \tag{2.13}$$

Notice that, to guarantee perfect voltage tracking it suffices to force the combined current i_m to follow a reference signal $\bar{i}_m$ given by (2.13), which, unfortunately, depends on the unavailable signal i_0 and unknown parameter C. Here, and in what follows $(\cdot)^*$ will be used to denote references and $\overline{(\cdot)}$ for values in the equilibrium.

Notice that the time derivative of the voltage reference, that is used later in the design process, is given by $\dot{v}^*_C = \mathcal{J}w_0v^*_C$.

3. PROPOSED CONTROLLER

3.1 Introduction

THE design of the proposed controller is based on the combined measurement of capacitor and load currents in the same current sensor arrangement. As pointed out before, the idea is, on the one hand, to reach a similar performance as that obtained in a capacitor current based controller, and on the other hand, to obtain a simple estimator for the inductor current which is used for security purposes only. A key idea in the design process is the description of the periodic disturbances in terms of their frequency domain variables, which include both symmetric components, namely, the negative and positive sequence for each harmonic component, thus, allowing the treatment of unbalance operation. By using the frequency domain descriptions of the disturbance signals, the solution presented here is able to perform precise voltage tracking despite of the presence of distorting loads. In terms of control theory, the proposed controller realizes a partial inversion of the system, and adds the needed damping. The resulting system contains a disturbance term due to the uncertainty in the system parameters which is then addressed via adaptation. An important observation is that, thanks to appropriate rotations, it is possible to reduce considerably the complexity of the proposed controller. Its final expression is very close to the conventional one, to which a bank of resonant filters have been added. The latter is constitutes one of the major contributions of the present work. It is interesting to mention that the introduction of the bank of resonant filters in agreement with the internal model principle. Moreover, the proposed controller com-

pensates only for a selected group of harmonic components, and thus, belongs to the family of selective control algorithms.

3.2 Controller design - the known parameters case

Let us write the dynamics of the system (2.8)-(2.9) in terms of the combined current i_m (2.10); this yields

$$L\frac{di_m}{dt} = -\alpha v_C - (\alpha-\beta)L\frac{di_0}{dt} + \frac{\alpha E}{2}u \tag{3.1}$$

$$\alpha C\frac{dv_C}{dt} = i_m - \beta i_0 \tag{3.2}$$

Notice that, the above system is a linear time invariant (LTI) system which is clearly controllable according to standard theory (see [26]).

The controller design is based on the following expression for the error model

$$\begin{aligned} L\frac{d\tilde{i}_m}{dt} &= -\alpha\left(\tilde{v}_C + v_C^*\right) + \alpha\frac{E}{2}u - (\alpha-\beta)L\frac{di_0}{dt} - L\frac{d\bar{i}_m}{dt} \\ &= \alpha\left(\frac{E}{2}u - \tilde{v}_C - v_C^*\right) - (\alpha-\beta)L\frac{di_0}{dt} - L\frac{d\bar{i}_m}{dt} \end{aligned} \tag{3.3}$$

$$\begin{aligned} \alpha C\frac{d\tilde{v}_C}{dt} &= \tilde{i}_m + \bar{i}_m - \beta i_0 - \alpha C\frac{dv_C^*}{dt} \\ &= \tilde{i}_m \end{aligned} \tag{3.4}$$

where the error variables are defined as $\tilde{v}_C \stackrel{\triangle}{=} v_C - v_C^*$ and $\tilde{i}_m \stackrel{\triangle}{=} i_m - \bar{i}_m$, with v_C^*, and $\bar{i}_m$ as defined in Chapter 2, and the fact that $\frac{dv_C^*}{dt} = \mathcal{J}w_0 v_C^*$ are used.

In the case of known parameters, i.e., with L, C, i_0 and $\frac{di_0}{dt}$ all known, the following controller that can be proposed to guarantees asymptotic stable tracking, that is, $\tilde{v}_C \to 0$ as $t \to \infty$.

$$\frac{\alpha E}{2}u = -R_1\tilde{i}_m - R_2\tilde{v}_C + (\alpha-\beta)L\frac{di_0}{dt} + \alpha v_C^* + L\frac{d\bar{i}_m}{dt},$$

where R_1 and R_2 are two positive design parameters to add the required damping. The design of the previous controller can be resumed as follows. First, a copy of the system is constructed and evaluated in the desired steady state. Second, we add to

that expression the required damping by feeding back the errors through the gains R_1 and R_2. Finally, from the resulting expression, we solve for the controller u. See [27] for further details in the passivity-based control design technique. Notice that most terms of the controller above are intended to cancel the corresponding terms in the error model.

3.3 Controller design - the unknown parameters case

Now, in the case that the system parameters and disturbances are unknown, the following controller based on the structure of the above controller is proposed .

$$\frac{\alpha E}{2}u = -R_1(i_m - i_m^*) - R_2\tilde{v}_C + (\alpha-\beta)\hat{L}\frac{d\hat{i}_0}{dt} + \alpha v_C^* + \hat{L}\frac{di_m^*}{dt} \tag{3.5}$$

where $\widehat{(\cdot)}$ is used to represent the estimated value of $(\cdot)$, and we have replaced $\bar{i}_m$ by $i_m^* \triangleq \alpha\mathcal{J}w_0\hat{C}v_C^* + \beta\hat{i}_0$, which is a signal used to approximate $\bar{i}_m$, since C is a unknown parameter and i_0 is not available. Notice that in this controller all unknown terms have been replaced by their estimates.

The main idea behind the controller design consists in lumping all periodic uncertainties in a single term $\hat{\phi}$ as follows

$$\frac{\alpha E}{2}u = -R_1 i_m - R_2\tilde{v}_C + \alpha v_C^* + \hat{\phi} \tag{3.6}$$

where $\hat{\phi} = R_1 i_m^* + (\alpha-\beta)\hat{L}\frac{d\hat{i}_0}{dt} + \hat{L}\frac{di_m^*}{dt}$. The relevance of this representation will be more evident later on.

Direct substitution of (3.5) in the system (3.3)-(3.4) yields the closed loop system

$$\begin{aligned}
\frac{L d\tilde{i}_m}{dt} &= -R_1\tilde{i}_m - (\alpha+R_2)\tilde{v}_C + \underbrace{\left(R_1 i_m^* + (\alpha-\beta)\hat{L}\frac{d\hat{i}_0}{dt} + \hat{L}\frac{di_m^*}{dt}\right)}_{\hat{\phi}} \\
&\quad - \underbrace{\left(R_1\bar{i}_m + (\alpha-\beta)L\frac{di_0}{dt} + L\frac{d\bar{i}_m}{dt}\right)}_{\bar{\phi}} \\
&= -R_1\tilde{i}_m - (\alpha+R_2)\tilde{v}_C + (\hat{\phi}-\bar{\phi}) \qquad (3.7) \\
\alpha C\frac{d\tilde{v}_C}{dt} &= \tilde{i}_m \qquad (3.8)
\end{aligned}$$

where $\overline{\phi} \triangleq R_1\bar{i}_m + (\alpha-\beta)L\frac{di_0}{dt} + L\frac{d\bar{i}_m}{dt}$ have been defined.

Notice that this system, referred as the *error dynamics*, is a system LTI perturbed by a periodic disturbance $(\hat{\phi}-\overline{\phi})$. Moreover, it is easy to see that the system above satisfy the so called *matching condition*, therefore the perturbation $\overline{\phi}$ can be cancelled by means of the actual control $\hat{\phi}$ (see [28]).

3.4 Disturbance rejection

According to (2.11) the periodical signals $\hat{\phi}$ and $\overline{\phi}$ can be described as follows

$$\begin{aligned}\hat{\phi} &\triangleq \sum_{k\in\mathcal{H}}\left(\hat{\phi}_k^p + \hat{\phi}_k^n\right) = \sum_{k\in\mathcal{H}}\left(e^{\mathcal{J}w_0kt}\hat{\Phi}_k^p + e^{-\mathcal{J}w_0kt}\hat{\Phi}_k^n\right)\\ \overline{\phi} &\triangleq \sum_{k\in\mathcal{H}}\left(\phi_k^p + \phi_k^n\right) = \sum_{k\in\mathcal{H}}\left(e^{\mathcal{J}w_0kt}\Phi_k^p + e^{-\mathcal{J}w_0kt}\Phi_k^n\right)\end{aligned}$$

where the vectors Φ_k^p, $\Phi_k^n \in \mathbb{R}^2$ are the k-th harmonic coefficients for the positive and negative sequence representation of the disturbance $\overline{\phi}$, and $\hat{\Phi}_k^p$, $\hat{\Phi}_k^n$ their corresponding estimates.

As a result the error signal $\tilde{\phi} = (\hat{\phi}-\overline{\phi})$ can be expressed as

$$\tilde{\phi} \triangleq \sum_{k\in\mathcal{H}}\left(\tilde{\phi}_k^p + \tilde{\phi}_k^n\right) = \sum_{k\in\mathcal{H}}\left(e^{\mathcal{J}w_0kt}\tilde{\Phi}_k^p + e^{-\mathcal{J}w_0kt}\tilde{\Phi}_k^n\right)$$

where $\tilde{\Phi}_k^p \triangleq (\hat{\Phi}_k^p - \Phi_k^p)$ and $\tilde{\Phi}_k^n \triangleq (\hat{\Phi}_k^n - \Phi_k^n)$ are defined.

The adaptive laws are obtained by following a Lyapunov approach where the proposed energy storage function is

$$W = \frac{\alpha LC|\dot{\tilde{v}}_C|^2}{2} + \frac{(\alpha+R_2)|\tilde{v}_C|^2}{2} + \sum_{k\in\mathcal{H}}\frac{\left[(\tilde{\Phi}_k^p)^2 + (\tilde{\Phi}_k^n)^2\right]}{2\gamma_k} \tag{3.9}$$

where γ_k, $k\in\mathcal{H}$, are positive design constants.

Its time derivative along the trajectories of (3.8) gives

$$\dot{W} = -\alpha R_1 C\dot{\tilde{v}}_C^2 + \dot{\tilde{v}}_C^\top\sum_{k\in\mathcal{H}}\left[e^{\mathcal{J}kw_0t}\tilde{\Phi}_k^p + e^{-\mathcal{J}kw_0t}\tilde{\Phi}_k^n\right] + \sum_{k\in\mathcal{H}}\frac{\left[(\dot{\tilde{\Phi}}_k^p)^\top\tilde{\Phi}_k^p + (\dot{\tilde{\Phi}}_k^n)^\top\tilde{\Phi}_k^n\right]}{\gamma_k}$$

which is made negative semidefinite by proposing the following adaptation laws

$$\dot{\hat{\Phi}}_k^p = -\gamma_k e^{-\mathcal{J}kw_0t}\dot{\tilde{v}}_C \quad , \quad \dot{\hat{\Phi}}_k^n = -\gamma_k e^{\mathcal{J}kw_0t}\dot{\tilde{v}}_C \tag{3.10}$$

where $\dot{\hat{\Phi}}_k^p = \dot{\tilde{\Phi}}_k^p$ and $\dot{\hat{\Phi}}_k^n = \dot{\tilde{\Phi}}_k^n$ since Φ_k^p and Φ_k^n are assumed constant.

Since $\dot{W} = -\alpha R_1 C\dot{\tilde{v}}_C^2$, as a first conclusion we have that $\dot{\tilde{v}}_C \to 0$ and moreover it is bounded. Then invoking standard LaSalle's theorem arguments [29] assuming $\dot{\tilde{v}}_C \equiv 0$ in the closed loop system (3.7) and (3.8), the invariant set described by $(\alpha + R_2)\tilde{v}_C = \tilde{\phi}$ is obtained; in addition $\hat{\Phi}_k^p$, $\hat{\Phi}_k^n$ are constant $\forall k \in \mathcal{H}$, which implies in turn that $\tilde{\phi}$ is a time varying bounded signal. However, $\tilde{v}_C$ is a constant and bounded signal, therefore, the only possible solution is $\tilde{v}_C \to 0$ which in turn implies $\tilde{\phi} \to 0$, and moreover $\tilde{\Phi}_k^p \to 0$ and $\tilde{\Phi}_k^n \to 0$.

Summarizing, the controller composed by (3.6) and (3.10) guarantees tracking of the capacitor voltage towards its sinusoidal reference despite of the presence of a distorted load current, that is, with disturbance rejection. In what follows it is shown that, by means of suitable rotations, it is possible to reduce considerably the expression and computational effort of the proposed controller, thus facilitating its implementation.

3.5 Controller simplification

To facilitate the implementation of the above controller the following transformations (rotations) are proposed

$$\hat{\phi}_k^p = e^{\mathcal{J}kw_0t}\hat{\Phi}_k^p \quad , \quad \hat{\phi}_k^n = e^{-\mathcal{J}kw_0t}\hat{\Phi}_k^n. \tag{3.11}$$

Thus the adaptation laws can be written as

$$\dot{\hat{\phi}}_k^p = -\gamma_k\dot{\tilde{v}}_C + \mathcal{J}kw_0\hat{\phi}_k^p \tag{3.12}$$

$$\dot{\hat{\phi}}_k^n = -\gamma_k\dot{\tilde{v}}_C - \mathcal{J}kw_0\hat{\phi}_k^n. \tag{3.13}$$

The transfer function expressions of the adaptation laws are given by

$$\hat{\phi}_k^p = \frac{-\gamma_k s(s + \mathcal{J}kw_0)}{s^2 + k^2w_0^2}\tilde{v}_C$$

$$\hat{\phi}_k^n = \frac{-\gamma_k s(s - \mathcal{J}kw_0)}{s^2 + k^2 w_0^2}\tilde{v}_C$$

where s is the complex variable.

Therefore the adaptations are reduced to

$$\begin{aligned}\hat{\phi}_k &= \hat{\phi}_k^p + \hat{\phi}_k^n = \frac{-2\gamma_k s^2}{s^2 + k^2 w_0^2}\tilde{v}_C \\ &= -2\gamma_k \tilde{v}_C + \frac{2\gamma_k k^2 w_0^2}{s^2 + k^2 w_0^2}\tilde{v}_C \ . \end{aligned} \tag{3.14}$$

In conclusion, the final expression for the controller is given by

$$\frac{\alpha E}{2}u = -R_1 i_m - \left(R_2 + 2\sum_{k\in\mathcal{H}}\gamma_k\right)\tilde{v}_C + \alpha v_C^* + \sum_{k\in\mathcal{H}}\frac{2\gamma_k k^2 w_0^2}{s^2 + k^2 w_0^2}\tilde{v}_C. \tag{3.15}$$

Figure 3.1 presents the block diagram of the final proposed controller (3.15). Notice that this structure is composed of: a proportional term acting over the combined current i_m aimed to add the required damping; a term α multiplying the reference voltage v_C^*, which is intended to keep the natural damping when added to the corresponding term αv_C appearing in the model description (3.1)-(3.2); a proportional term acting over the voltage error $\tilde{v}_C$ to improve the required damping, notice that, this term depends on the γ_k value, therefore special care should be taken to update this term when the harmonic compensation is enabled; a bank of resonators of the form $\frac{2\gamma_k k^2 w_0^2}{s^2+k^2 w_0^2}$, $\forall k \in \mathcal{H}$ acting over the voltage error $\tilde{v}_C$. This bank of resonant filters is dedicated to the harmonic compensation.

For comparison, a simple controller that captures the essence of the multiple reported capacitor current based controllers [17], [18], [20] has been drawn in Fig. 3.2 to exhibit the main differences with respect to the proposed controller. This simple controller is referred in this work as the conventional controller, which is composed of the following terms: a proportional term acting over i_C to add the required damping; the reference voltage v_C^*, which is referred as the feedforward term; a proportional term acting over $\tilde{v}_C$ to add the required damping. Notice that, this controller does not contain a term specifically devoted to the harmonic compensation. Some authors prefer to use $\tilde{i}_C$ instead of i_C, for this, they introduce a reference i_C^* which requires the time derivative of the reference v_C^*, plus the knowledge of the capacitance. Yet some

authors introduce the second time derivative of the capacitor voltage reference affected by the inductance and capacitance with the aim to improve the tracking. But all this terms complicate the controller expression and are very sensitive to system parameters variations. Anyway, none of these proposals solve the disturbance rejection issue stated here.

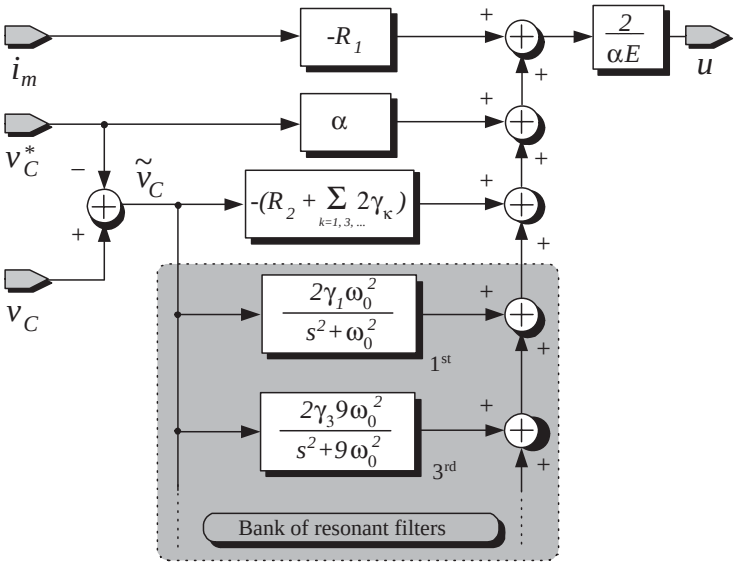

Fig. 3.1: Block diagram of the proposed controller.

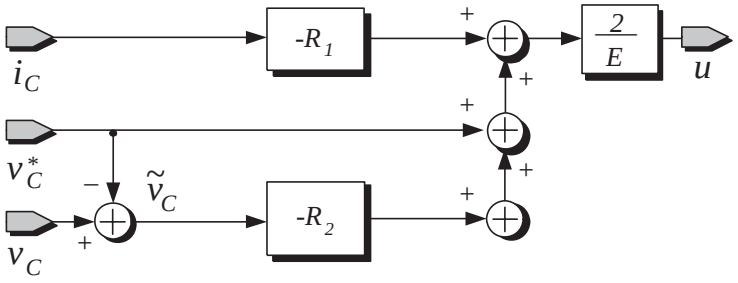

Fig. 3.2: Block diagram of the conventional controller.

3.6 Estimation of the inductor current i_L

As pointed out before, the aim of the proposed combined current arrangement is the facility to reconstruct the inductor current i_L which can then be used for protection purposes only. Solving for i_L from (2.9)-(2.10) yields

$$i_L = \frac{1}{\beta} i_m + \frac{\beta - \alpha}{\beta} i_C \tag{3.16}$$

which unfortunately requires the unaccessible signal i_C. However, since the capacitor current i_C is defined as C times the time derivative of the capacitor voltage v_C, it is possible to estimate i_L as follows

$$\hat{i}_L = \frac{1}{\beta} \left(\frac{1}{\sigma s + 1} \right) i_m + \frac{\beta - \alpha}{\beta} \left(\frac{Cs}{\sigma s + 1} \right) v_C \tag{3.17}$$

where $\hat{i}_L$ represents the estimate of i_L. The idea behind this estimator consists in introducing a LPF with a pole fixed at $1/\sigma$ on the right hand side of (3.16). This produces a proper filter to reconstruct i_C using v_C which is the accessible signal. Notice that such a proper filter is basically a time derivative operator with a limited bandwidth fixed by $1/\sigma$, which is also referred in control literature as "dirty" (or approximate) time derivative. The bandwidth is selected big enough to guarantee a good tracking of i_C. Since the higher order harmonics in i_C have been truncated in $\hat{i}_C$, due to the limited bandwidth of the estimator, then, also the higher order harmonics of i_m should be eliminated before computation of $\hat{i}_L$ in (3.17) to avoid unnecessary distortion. The estimate of i_L can now be used in a surveillance block to guarantee a safer operation of the inverter system.

Remark 3.6.1 It is clear that a much smaller β compared to α would produce a faster response, as i_m is dominated mainly by i_C, however, it was observed from (3.17) that extremely low values of β makes the above estimator very sensitive to variations on parameter C. Thus, values for parameters α and β should be carefully selected to establish a tradeoff between speed response and sensitivity. □

4. PHYSICAL IMPLEMENTATION

4.1 Introduction

AN UPS prototype has been built to experimentally prove the proposed controller and estimator developed in Chapter 3. The power stage of the UPS system is built using a VSI produced by SEMIKRON under the commercial name *"Power Electronics Teaching System"*. To eliminate the switching effect of the devices a smoothing LC filter is connected at the output of the VSI. A three phase diode rectifier feeding a resistor, plus a resistor connected in between two phases to produce unbalance are used as the distorted unbalanced load. The load is connected and disconnected from the UPS by means of a set of relays controlled from the computer.

For the instrumentation of the inverter prototype we have introduced sensors, signal conditioners, voltage limiters and a control interface. The proposed controller and estimator have been implemented in a digital signal processor (DSP) based card $ACE1103$ made by dSPACE. This same card also performs the analog-to-digital (AD) conversion. The UPS system, the instrumentation stages and the proposed control are shown in Fig. 4.1.

The sensors and corresponding signal conditioners have been placed in the same card and communicated to the dSPACE card via a set of voltage limiters to protect the acquisition ports of the dSPACE. The sensed signals are the combined currents i_{m123} and the capacitor voltages v_{C123}. The used sensors provide galvanic isolation.

The controller has been programmed using the environment Simulink/MATLAB, and then compiled and downloaded to the dSPACE card using the Realtime-Workshop tools included in Simulink package. The principal steps are described next: First, the sensed signals are transformed from 123-coordinates to $\alpha\beta$-coordinates, which are the feedback signals used in the proposed controller. Once the control signal u is computed, it is transformed from $\alpha\beta$-coordinates to 123-coordinates. This control signal is then mapped back to the duty cycle d_{123}, which is then injected in the SPWM to generate the switching sequence δ_{123}.

The control interface card communicates digital signals between the control stage, i.e., the dSPACE card, and the drivers feeding the gates of the power devices in the VSI. This card provides galvanic insolation between the dSPACE card and the drivers. The control interface is able to interrupt the SPWM switching sequence, if over current or over voltage conditions appear.

4.2 Power stages

4.2.1 Three-phase three-wire UPS system

The *"Power Electronics Teaching System"* from SEMIKRON includes a three-phase diode rectifier SKD-51/14, a pair of capacitors of 2200 μF, three drivers SKHI-22A and three half-bridge modules SKM50-GB123D implemented with IGBT and free-wheeling diode.

Figure 4.2 shows the implemented electric diagram for this stage. The input voltage E has been obtained using the rectifier SKD-51/14 and the pair of capacitors of 2200 μF are connected in series. The driver SKHI-22A protects the IGBTs against short circuit and low power supply voltage. Each of the drivers SKHI-22A controls an inverter leg and provides an error signal (Error 1, Error 2 and Error 3) of negative logic, i.e., it gives a 15 V signal when there is no error. If an error condition is detected, the driver stops and the input impulses are ignored. The resetting of the error latch is achieved by forcing both inputs to zero, and suppressing the cause of the error. The drivers are independent from each other, therefore it is necessary to take

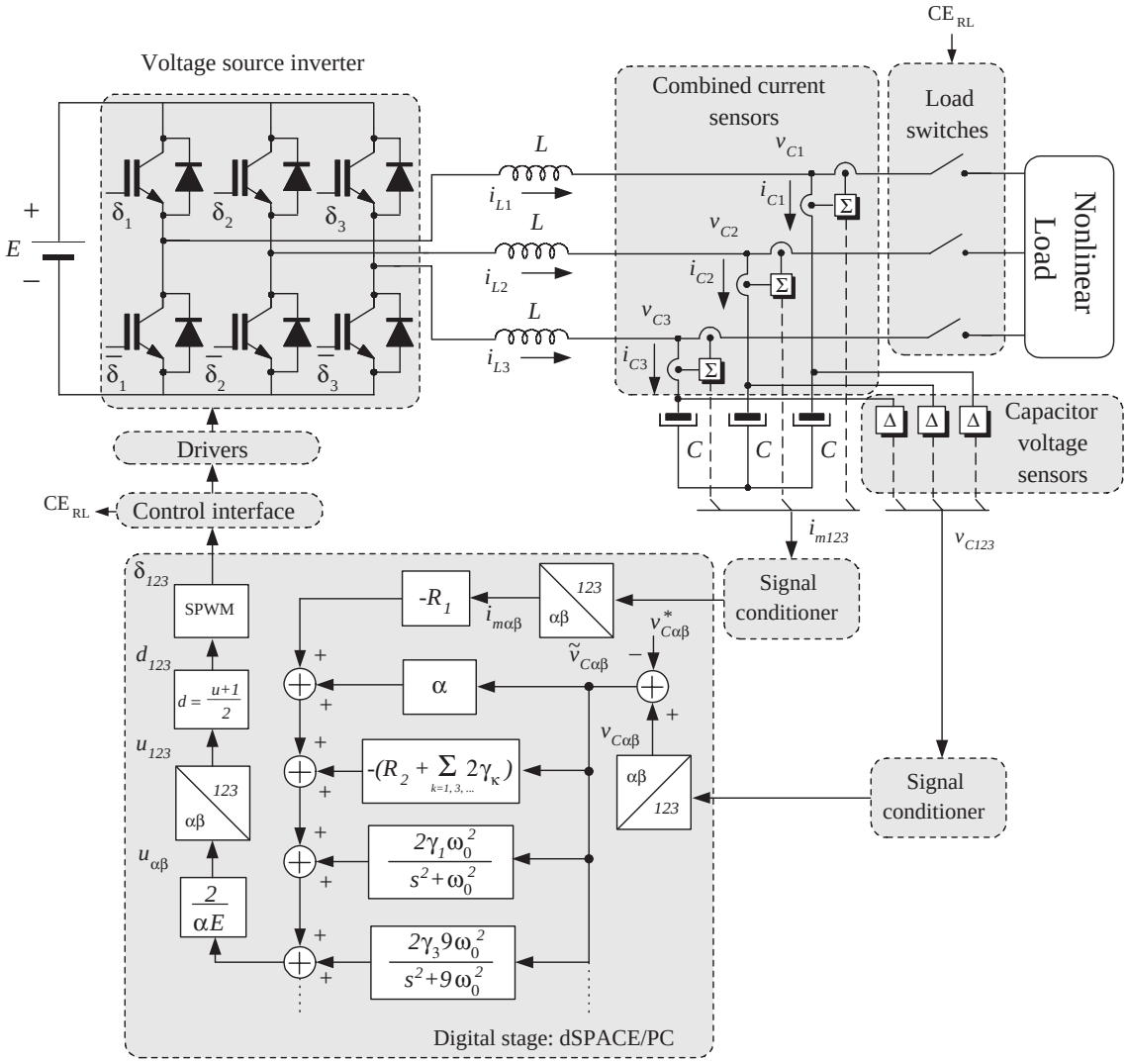

Fig. 4.1: General scheme of the UPS system with proposed control and instrumentation stages.

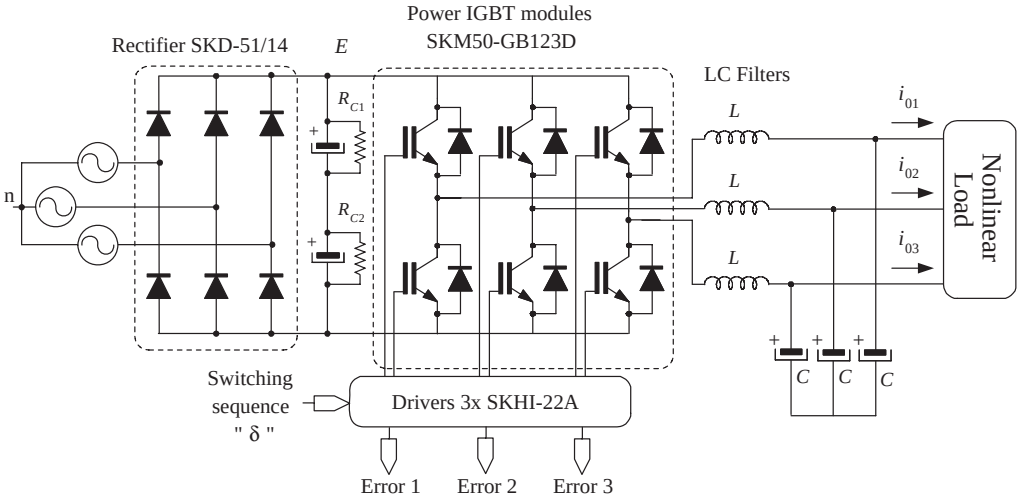

Fig. 4.2: Three-phase three-wire UPS system.

all the precautions to shut the system off when an error condition is sensed. All these precautions have been considered in the control interface card, which is described below. Each module SKM50-GB123D represents an inverter leg made of two IGBT, with antiparallel diode, connected in series. The IGBTs turned on, i.e., they conduct, if a 15 V signal is placed between gate and emitter, and they are turned off if a -15 V signal is placed instead. These control signals are delivered by the SKHI-22A, through an additional gate resistor of 30 Ω. Finally, the cut-off frequency of the output LC filter has been placed at approximately 1Khz, that is, a decade below the switching frequency. The parameters used in the UPS prototype system are collected in Table 4.1.

4.2.2 Distorted unbalanced load

The nonlinear load is composed of a three-phase diode rectifier PSD-31/12 connected to a DC capacitor of 235 μF feeding a resistor of 100 Ω. To produce the unbalance condition a resistor of 150 Ω is connected in between two phases. Figure 4.3 shows the implemented electrical circuit for the unbalanced nonlinear load. The elements used in the distorted unbalanced load are collected in Table 4.1. Figure 4.4 shows (top plot) the time response for one of the measured load currents, and (bottom plot) its

corresponding frequency spectrum. Notice that the load current is composed mainly by odd harmonics of the fundamental f_0, mainly 1st, 3rd, 5th and 7th components. These harmonics are precisely the components considered for compensation, that is, the bank of resonant filters includes filters tuned at 1st, 3rd, 5th and 7th harmonic of the fundamental f_0.

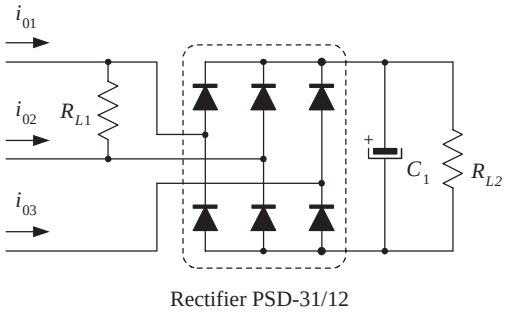

Fig. 4.3: Distorted unbalanced load.

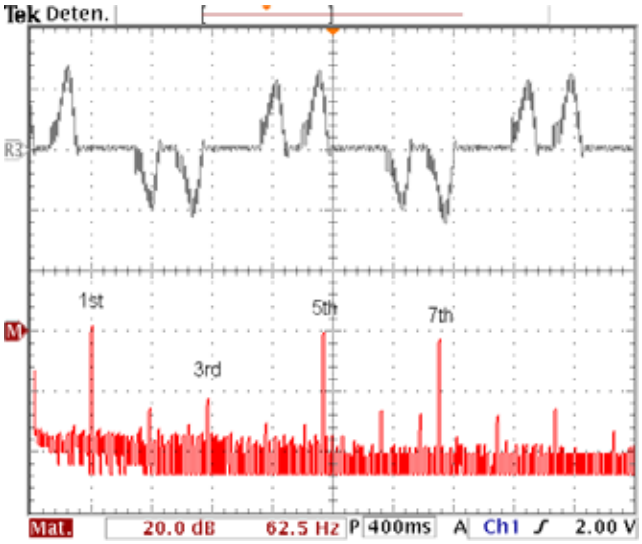

Fig. 4.4: Load current (only one phase): **(top)** the current signal i_{01} in the time domain (x-axis 200 ms/div, y-axis 5 A/div) and **(bottom)** its corresponding frequency spectrum (x-axis 62.5 Hz/div, y-axis 20 dB/div).

4.4.3 Load switches

In the experimental results, it is necessary to obtain the transient response during the connection and disconnection of the load. This task is performed via a set of three relay switches, one for each phase, controlled from the computer. Figure 4.5 shows the implemented electrical circuit for the relay switches and their corresponding drivers. The buffer $IC7.1$ reinforces the CE_{RL} signal (this buffer is the same integrated circuit used in the control interface). The optocoupler $IC15.1$ provides galvanic insolation between the buffer and the inductor of the power relay $T92$. The resistances R_{29} and R_{30} limits the current across from the transistor of $IC15.1$. The diode D_5 permits the current to flow only on the direction towards the transistor Q_1. The diode D_4 deviates the inverse current produced by the bobbin of the power relay during the turn off. The light emitter diode D_3 indicates the actual state of the power relay. Notice that, if the dSPACE control signal is the logic OFF, the transistor of the $IC15.1$ and the transistor Q_1 do not conduct, while if it is ON, both transistors conduct activating the bobbin of the power relay, allowing the output current to flow. The devices used in the relay based load switches are collected in Table 4.1.

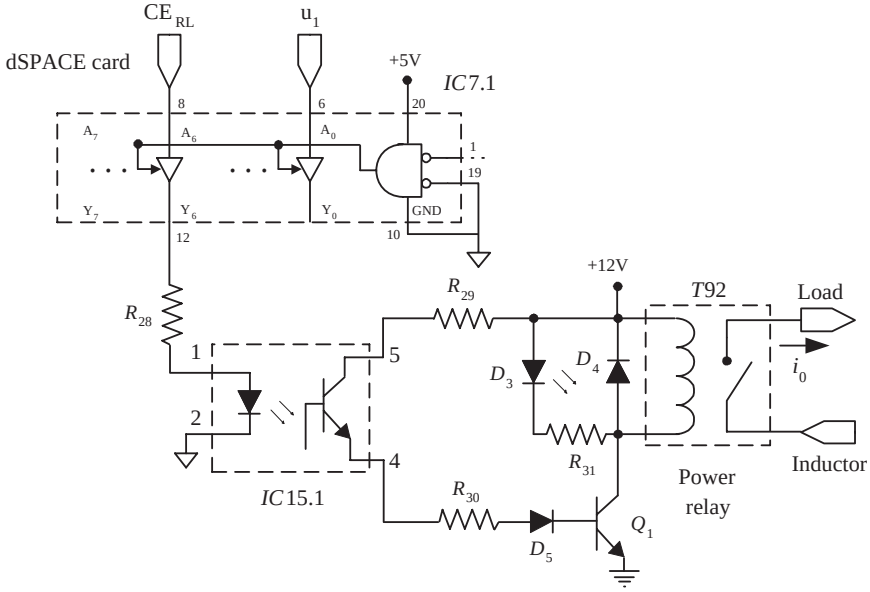

Fig. 4.5: Electric circuit of the load switches.

L	:	1mH
C	:	25μF
C_1	:	235μF
R_{L1}	:	150Ω
R_{L2}	:	100Ω
R_{C1}, R_{C2}	:	22kΩ
R_{28}	:	330Ω
R_{29}, R_{31}	:	2.2kΩ
R_{30}	:	220Ω
D_4, D_5	:	1N4937
Q_1	:	BC548
$IC15.1$	:	CNY17-2
IGBTs	:	SKM50-GB123D
Light emitter diode	:	D_3
Power relay	:	$T92$
Rectifier of input voltage	:	SKD-51/14
Rectifier of load	:	PSD-31/12
Drivers	:	SKHI-22A

Table 4.1: Devices and parameters of the power stages.

4.3 Sensors and signal conditioning stages

4.3.1 Combined current sensor arrangement

As it was mentioned, the proposed controller as well as the proposed observer have been implemented with the dSPACE card. Therefore, the combined current sensor should provide isolation between the power stage and the dSPACE based controller card. Moreover, it is necessary to limit such signals (one for each phase) to the admissible range [-10V, 10V] prior to send them to the analogical digital ports (ADP) of the dSPACE. Figure 4.6 shows the implemented electric circuit for the mixed current sensor. The mixed current is sensed with the current sensor CLN-50. This

sensor provides electric isolation between the current carrying conductor(s) and the control circuit. The sensor CLN-50 is a closed-loop Hall effect current sensor that accurately measures DC and AC currents. In the CLN-50 both conductors, the one conducting the capacitor current and the other conducting the load current, have been wired as to obtain $\alpha = 10$ and $\beta = 1$, that is, we have given 10 turns of the former and 1 turn for the latter. The sensor thus, furnishes directly the weighted sum of both currents. The operational amplifier $IC1.1$ is connected as *current-to-voltage converter*, i.e., the $IC1.1$ provides a proportional voltage to the mixed current. The $IC2.1$ regains the sign of the mixed current. The transfer function of the delivered voltage v_{im} is given by expression (4.1). The devices and parameters used in the combined current sensor circuit are collected in Table 4.2. Figure 4.7 shows a picture of the implemented cards.

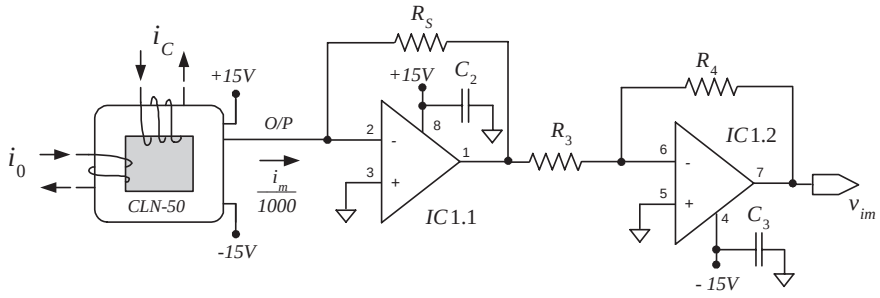

Fig. 4.6: Electric circuit of the combined current sensor.

$$v_{im} = 1 \times 10^{-3} \frac{R_4}{R_3} R_S i_m \tag{4.1}$$

4.3.2 Capacitor voltage sensor

In the same form as in the combined current sensor, the capacitor voltage sensor should provide galvanic isolation between the power stage and the control circuit. Moreover, these capacitor voltage signals (one for each phase) should be limited prior to send them to the analogical digital converters (ADCs) in the dSPACE card. Figure 4.8 shows the implemented electric circuit for this stage. The transformer gives galvanic isolation between the capacitor voltage and the control stage. It also reduces

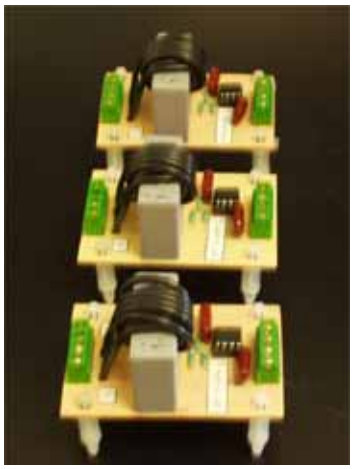

Fig. 4.7: Electric circuit of the combined current sensor.

R_S	:	50Ω
R_3	:	5kΩ
R_4	:	10kΩ
C_2, C_3	:	0.1μF
$IC1.1$, $IC1.2$	:	TL082
Current sensor	:	CLN-50

Table 4.2: Devices and parameters of the combined current sensor.

the voltages to allowed levels in the operational amplifiers $IC2.1$ and $IC2.2$. The operational amplifier $IC2.2$ regains the sign of the capacitor voltage. The transfer function of the delivered voltage v_{vc} is given by the expression 4.2. The devices and parameters used in the capacitor voltage sensor circuit are given in Table 4.3. Figure 4.9 shows a picture of the implemented cards.

$$v_{vc} = 0.1\frac{R_6 R_8}{R_5 R_7} v_C. \tag{4.2}$$

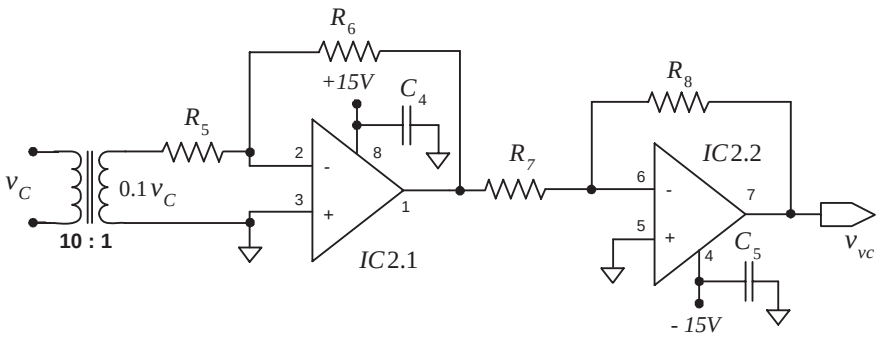

Fig. 4.8: Electric circuit of the capacitor voltage sensor.

Fig. 4.9: Electric circuit of the capacitor voltage sensor.

R_5, R_7, R_8	:	10kΩ
R_6	:	270kΩ
C_4, C_5	:	0.1μF
$IC2.1$, $IC2.2$	:	TL082

Table 4.3: Devices and parameters of the capacitor voltage sensor.

4.3.3 Limiting voltage interface card

The ADCs in the dSPACE card allow input voltages in the range $\pm 10V$, therefore, a limiting voltage card has been designed to guarantee that the sensor delivered voltages v_{im} and v_{vc} never exceed this range. Figure 4.10 shows the implemented electric diagram for this stage. The operational amplifier $IC3.1$ is connected as *noninverting voltage follower* serving as a coupling to the input signal. The resistor R_9 limits the current through $IC3.1$. The Zener diodes D_1 and D_2 keep the output voltage v_{ro} in the range $\pm 10V$. The devices and parameters used in the voltage limiter circuit are given in Table 4.4. Figure 4.11 shows a picture of the implemented card.

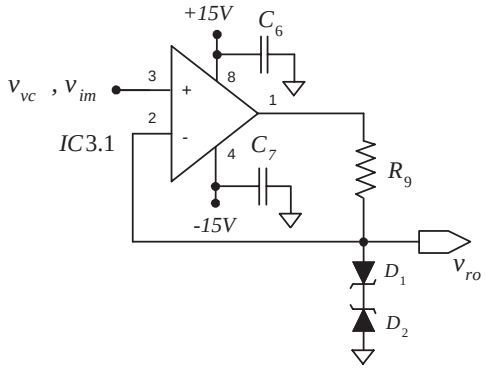

Fig. 4.10: Electric circuit of voltage limiter.

R_9	:	100Ω
C_6, C_7	:	0.1μF
D_1, D_2	:	IN4740A
$IC3.1$	:	TL082

Table 4.4: Devices and parameters used in the voltage limiter.

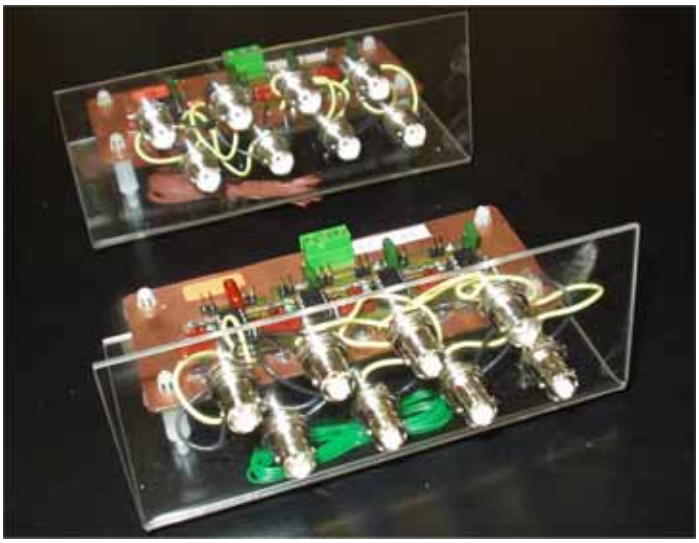

Fig. 4.11: Picture of the voltage limiter card.

4.3.4 Control interface

The control interface permits the transfer of the PWM switching sequences generated in the dSPACE card to the drivers SKHI-22A, providing galvanic isolation. In addition, this card protects the UPS system against short circuit and power supply low voltage condition, which is performed by interpreting the error signals of the drivers SKHI-22A (Error 1, Error 2 and Error 3) shown in Figure 4.2. Moreover, the control interface is able to interrupt the operation, by software, if conditions of over voltage or over current are detected in the power stage. Figure 4.12 shows the implemented electrical diagram for this card. The buffer $IC8.1$ reinforces the PWM switching and the chip enable (CE) digital signals coming from the dSPACE card. The buffer stops the input signals if any error condition is detected. The optocouplers

$IC4.1$, $IC5.1$ and $IC6.1$ provide galvanic insolation for the error signals produced in the drivers. The optocouplers $IC9.1$, $IC10.1$, $IC11.1$, $IC12.1$, $IC13.1$ and $IC14.1$ provide galvanic insolation for the PWM switching signals produced in the dSPACE control card. As it was mentioned, the drivers SKHI-22A provide a negative logic error signal, i.e., they give a 15V signal when no error has occurred. The NAND logic gate $IC8.1$ enables the buffer. Therefore, the conditions for the buffer to allow the transfer of the PWM switching signals, are if no error condition has been detected and if the CE signal is at a logical ON level. The devices and parameters used in the control interface card are given in Table 4.5.

R_{10}, R_{11}, R_{12}, R_{13}, R_{14}, R_{15}, R_{16}, R_{17}, R_{18}	:	2.2kΩ
R_{19}, R_{20}, R_{21}, R_{22}, R_{23}, R_{24}, R_{25}, R_{26}, R_{27}	:	2.2kΩ
C_8, C_9, C_{10}, C_{11}, C_{12}, C_{13}, C_{14}, C_{15}, C_{16}, C_{17}, C_{18}	:	0.1μF
$IC4.1$, $IC5.1$, $IC6.1$	:	HCPL-2211
$IC7.1$	:	SN74LS541N
$IC8.1$	:	SN74LS40N
$IC9.1$, $IC10.1$, $IC11.1$, $IC12.1$, $IC13.1$, $IC14.1$, $IC15.1$	:	HCPL-2211

Table 4.5: Devices and parameters used in the control interface.

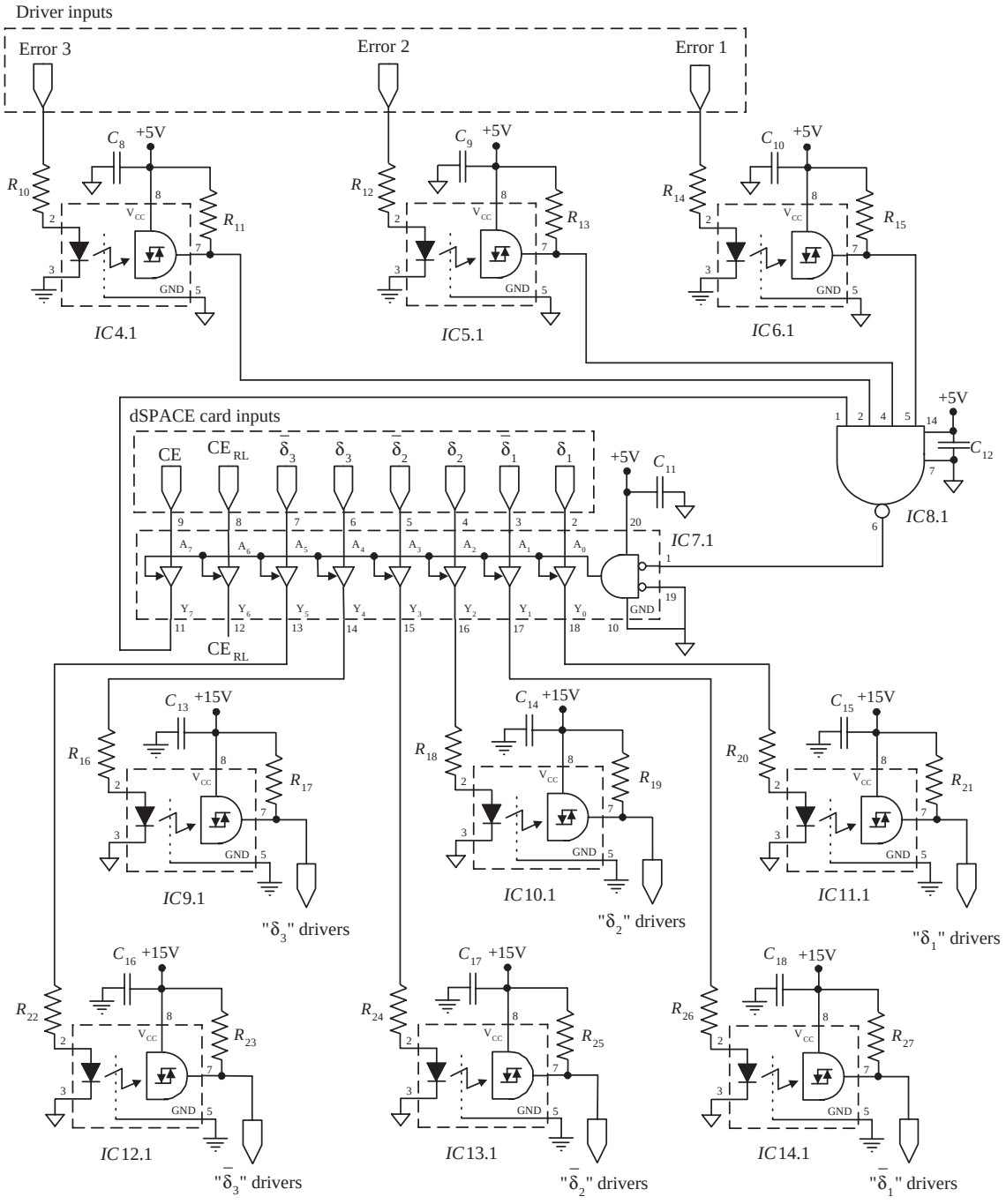

Fig. 4.12: Electric circuit of the control interface.

5. EXPERIMENTAL RESULTS

5.1 Introduction

THE proposed controller and the estimator developed in Chapter 3 have been tested in the three-phase three-wire UPS prototype whose design is explained in Chapter 4. As previously mentioned, the UPS prototype has been built using the following parameters: L = 1mH, C = 25μF, E = 320V, switching frequency f_{sw} = 10kHz, output voltage amplitude 110V with the fundamental frequency w_0 = 377r/s (f_0 = 60Hz). As pointed out before, the controller and the estimator are implemented in the dSPACE card model ACE1103 with a sampling rate fixed to 14.28kHz. In the controller, the resonant filters have been replaced by BPF to assure a safer operation. This is explained in detail in the next section, however the BPF are referred as resonant filters in the rest of this work. The bank of resonant filters includes filters tuned at 1st, 3rd, 5th and 7th harmonic of the fundamental w_0, i.e., these harmonics are the only components considered for compensation.

Different test have been carried out to assess the performance of the proposed controller and estimator. The tests include steady state responses and transient responses. The steady state responses include the measurements of the actual output voltage v_C, its reference v_C^*, the unbalanced load current i_0, and their corresponding frequency spectrums. These responses are compared with those of a conventional controller based on the capacitor current without harmonic compensation, to exhibit the performance improvements achieved with the proposed controller. Also, the actual

inductor current i_L is compared with its corresponding estimate $\hat{i}_L$. The transient responses include the measurements of v_C and i_0 during the connection and disconnection of the nonlinear load. Finally, voltage v_C, current i_L and its estimate $\hat{i}_L$ have been obtained during the turn off process of the inverter after the controller detects an inadmissible load condition.

5.2 Discussion on the resonant filters implementation

In order to guarantee a safer operation, BPF have been used instead of resonant filters. Recall that the latter have infinite gains at the resonant frequency, while the BPFs have limited gain due to a damping term introduced in the denominator of the transfer function as shown below

$$\frac{v_o}{v_i} = \frac{A_k k^2 w_0^2/Q_k}{s^2 + skw_0/Q_k + k^2 w_0^2} \quad \forall k \in \mathcal{H} \tag{5.1}$$

where A_k and Q_k are positive design parameters representing the desired gain and the quality factor of the k-th BPF, respectively; v_i and v_o are the input and output signals of the filter, respectively. Notice that, in the case of an ideal resonant filter $A_k \to \infty$. Therefore, the analytic function of the error dynamics model (3.7)-(3.8) and (3.14) is the following

$$\alpha LCs^2\tilde{v}_C + \alpha R_1 Cs\tilde{v}_C + (\alpha + R_2)\tilde{v}_C + \sum_{k\in\mathcal{H}} \left(-\frac{2A_k}{Q_k} + \frac{2A_k k^2 w_0^2/Q_k}{s^2 + skw_0/Q_k + k^2 w_0^2} \right) \tilde{v}_C = -\overline{\phi},$$

Notice that the resonant filters have been replaced by BPFs and the original gain γ_k in the resonant filters has been replaced by A_k/Q_k. Figure 5.1 shows the Bode plots of the above analytic function established from the periodic disturbance $(-\overline{\phi})$ to the output voltage error $\tilde{v}_C$. The design parameters of the controller were selected as follows: $R_1 = 0.5$, $R_2 = 0.5$, $A_1 = 40$, $Q_1 = 35$, $A_3 = 10$, $Q_3 = 20$, $A_5 = 10$, $Q_5 = 12$, $A_7 = 10$, $Q_7 = 12$. Figure 5.1 shows that the controller introduces notches centered at the odd harmonics under compensation, that is, at the 1st, 3rd, 5th and 7th, therefore, the effect of such harmonic components is practically eliminated on the output error. For comparison, the frequency response of the proposed controller without the bank of resonators (BPFs), i.e., without the harmonic compensation, has been included as well (in gray).

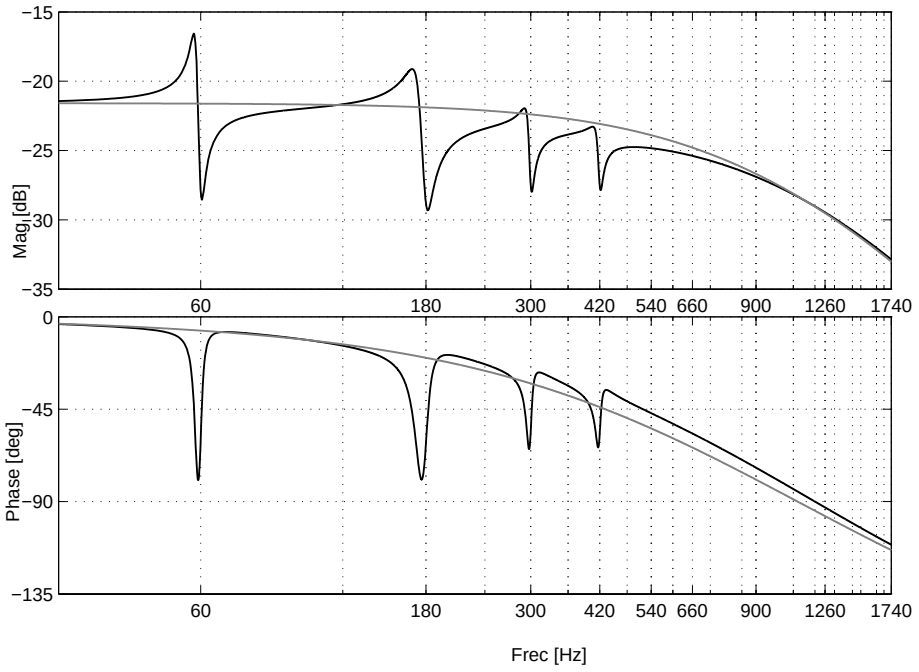

Fig. 5.1: Bode plot of the error dynamics ($-\overline{\phi} \mapsto \tilde{v}_C$) using the proposed controller **(black)** with harmonic compensation, and **(gray)** without the harmonic compensation: **(top)** Magnitude (x-axis in [Hz], y-axis in [dB]) and **(bottom)** phase shift (x-axis in [Hz], y-axis in [deg])

5.3 Steady state responses

Figure 5.2 shows, for one phase, (from top to bottom) the time responses of the output voltage reference v_C^*, the actual output voltage $v_C(t)$ and the tracking error $\tilde{v}_C(t)$, using the proposed controller based on i_m and with harmonic compensation. Notice that the actual voltage $v_C(t)$ (middle plot) is almost a pure sinusoidal signal and has an excellent tracking over its reference v_C^* (top plot), and thus the error $\tilde{v}_C(t)$ is made relatively small. The responses of the other two phases are very similar and are omitted here.

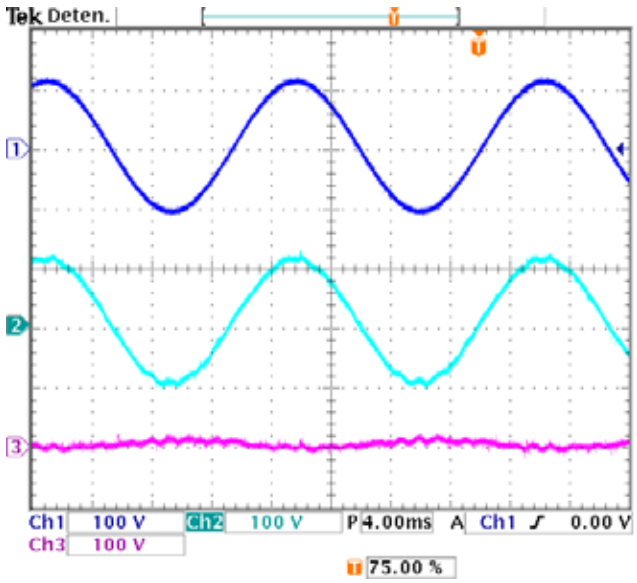

Fig. 5.2: Output voltage steady state response (only one phase) **(from top to bottom)** The reference voltage $v_C^*(t)$, the actual output voltage $v_C(t)$, and the error $\tilde{v}_C(t)$ (x-axis 4 ms/div, y-axis 100 V/div).

Figure 5.3 shows a comparison between the responses of the actual output voltage using the proposed controller (bottom plot), and a conventional controller using the measurement of i_C and without harmonic compensation (top plot). Notice that the performance of the proposed controller significantly exceeds that of the conventional one, even though for the latter, the gains have been adjusted to reach the best possible response. In the same plots the corresponding voltage references (in gray) have been included to put in evidence the better tracking reached with the proposed controller.

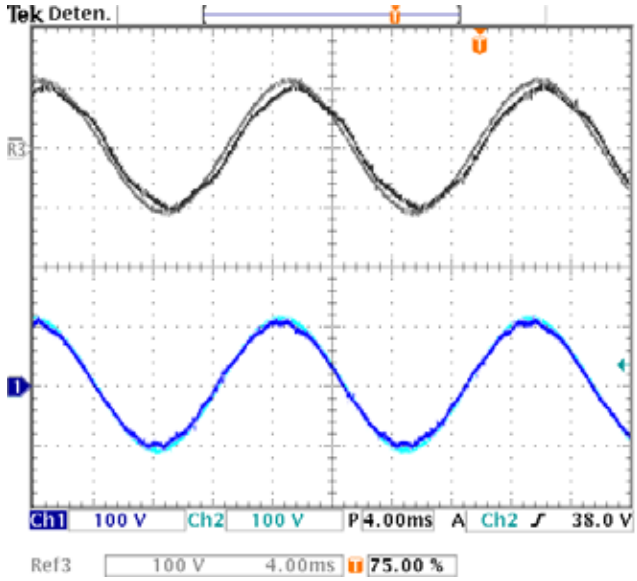

Fig. 5.3: Output voltage steady state response $v_C(t)$ in black, and corresponding reference $v_C^*(t)$ in gray (only one phase). **(top)** Conventional controller based on i_C measurements, and **(bottom)** proposed controller with harmonic compensation (x-axis 4 ms/div, y-axis 100 V/div).

Figure 5.4 shows the frequency spectrum of the output voltage for (top plot) the conventional controller and (bottom plot) the proposed controller. Notice that, in the proposed controller, the 3rd, 5th and 7th harmonic components have been eliminated almost completely thanks to the harmonic compensator. Table 5.1 shows the RMS voltage for each harmonic. Notice that in the proposed controller, the 3rd, 5th and 7th harmonic components have been considerably reduced in comparison to the conventional controller. As a consequence, the proposed controller has a better tracking, leading to an output voltage v_C mainly composed of the fundamental component despite the highly distorted load current. As shown in Table 5.1, the THD reached with the proposed controller is 1.16%, while that obtained with the conventional controller is 7.29%.

To compute the THD we have used the following expression (see [22]).

$$\%THD = 100 \times \frac{\left(\sum_{h=2}^{\infty} V_h^2\right)^{1/2}}{V_1}$$

where V_1 is the fundamental-frequency RMS value of the output voltage and V_h is the RMS magnitude at the harmonic of order h.

RMS voltage	$V_1[V_{RMS}]$	$V_3[V_{RMS}]$	$V_5[V_{RMS}]$	$V_7[V_{RMS}]$	$THD[\%]$
Conventional controller	100.05	1.77	7.07	0.79	7.29
Proposed controller	110	0	1.12	0.63	1.16

Table 5.1: Comparison of the THD reached with the proposed controller and with the conventional controller.

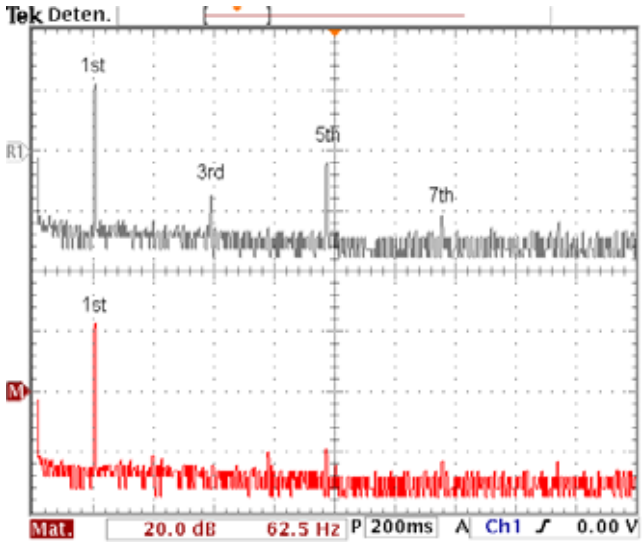

Fig. 5.4: Frequency spectrum of the output voltage $v_C(t)$ **(top)** Conventional controller based on i_C measurements, and **(bottom)** proposed controller with adaptable-based harmonic compensation (x-axis 62.5 Hz/div, y-axis 20 dB/div).

Figure 5.5 shows, for the proposed controller, the steady state response of the output voltages for the three phases v_{C1}, v_{C2}, v_{C3} (top plot), which are balanced and almost sinusoidal, despite of the distorted and unbalance load current. The last three plots present each of the three phase load currents i_{01}, i_{02}, i_{03}.

Figure 5.6 shows a detail of the current i_L and its estimate $\hat{i}_L$ in the steady state (only for one phase) using the estimator (3.17). Notice that the estimate $\hat{i}_L$ is very close to the actual current i_L, and thus it can be used for overcurrent protection purposes.

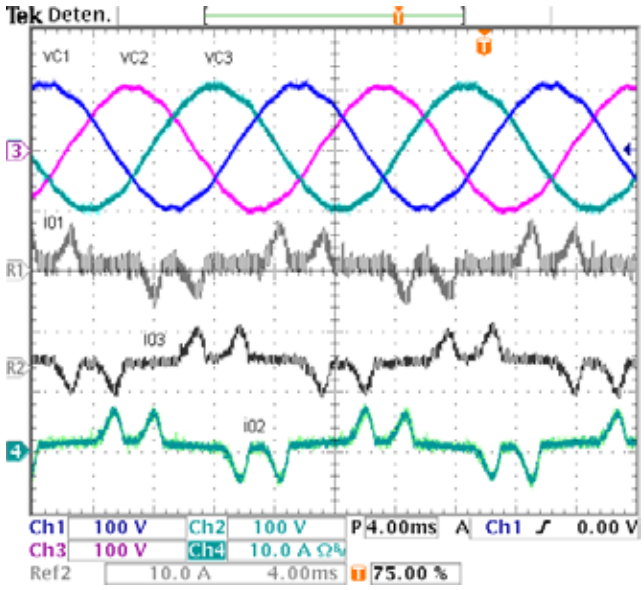

Fig. 5.5: **(top plot)** Steady state response of the three output voltages v_{C1}, v_{C2}, v_{C3} (x-axis 4 ms/div, y-axis 100 V/div) and **(three bottom plots)** distorted and unbalanced load currents i_{01}, i_{02}, i_{03} (x-axis 4 ms/div, y-axis 10 A/div).

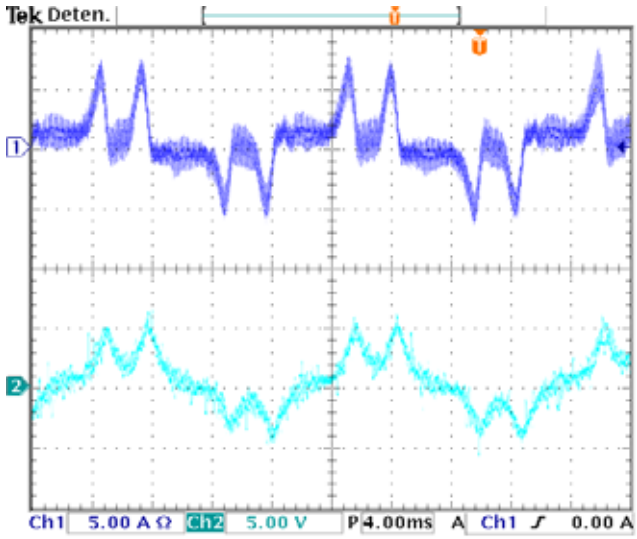

Fig. 5.6: **(top)** Actual inductor current i_L (x-axis 4 ms/div, y-axis 5 A/div) and **(bottom)** its estimate $\hat{i}_L$ (x-axis 20 ms/div, y-axis 5 V/div) (only one phase).

5.4 Transient responses

Figure 5.7 shows the transient response of the output voltage v_C (upper plot) when the nonlinear unbalanced load is connected to the inverter under the proposed controller. The corresponding current load i_0 is shown in the bottom plot (only one phase is shown for the sake of space limitations). Notice that after a relatively small transient the voltage keeps the desired sinusoidal shape and amplitude. Figure 5.8 shows the transient response after disconnecting the load.

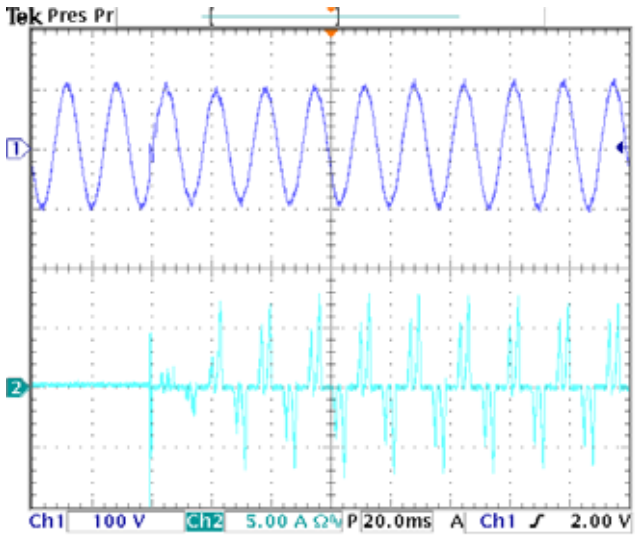

Fig. 5.7: Transient responses during the connection of the nonlinear and unbalanced load. **(top)** The output voltage v_C (x-axis 20 ms/div, 100 V/div) and **(bottom)** load current i_0 (x-axis 20 ms/div, y-axis 5 A/div).

Fig. 5.9 shows the transient responses of (from top to bottom) the output voltage v_C, the actual inductor current i_L and its estimate $\hat{i}_L$ during the turn off process of the inverter after the controller detects an inadmissible load condition. In this case, to test the usefulness of the estimate, a load is connected to the inverter demanding a current peak that surpasses the upper limit fixed at 8 A (only for experimental purposes). Once the controller realizes that the estimate $\hat{i}_L$ has gone beyond 8 A, the controller disables the switching process, zeroing the output voltage. Thanks to this action the semiconductor devices in the inverter are protected.

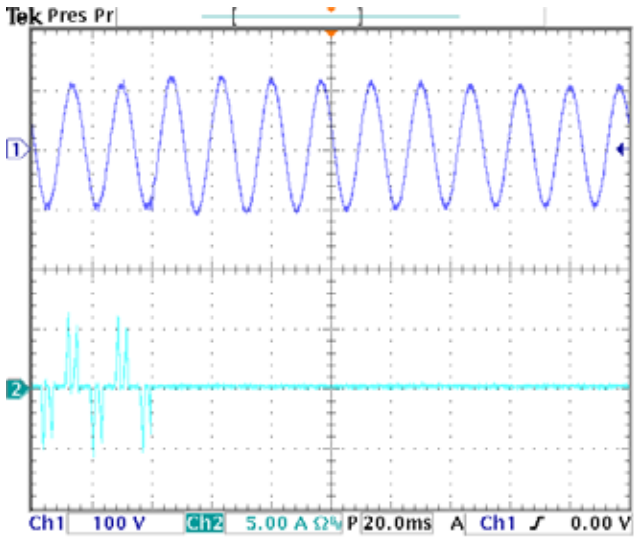

Fig. 5.8: Transient responses during the disconnection of the nonlinear and unbalanced load current. **(top)** The output voltage v_C (x-axis 20 ms/div, 100 V/div) and **(bottom)** load current i_0 (x-axis 20 ms/div, y-axis 5 A/div).

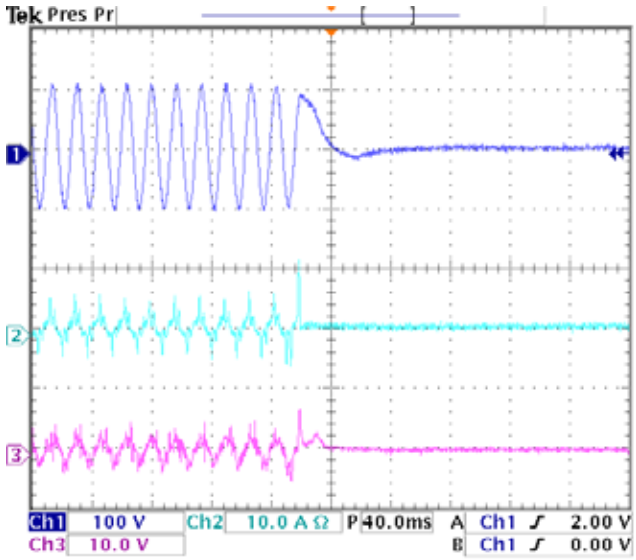

Fig. 5.9: Turn off process due to a load current amplitude exceeding the upper limit fixed at 8 A. **(from top to bottom)** The output voltage v_C (x-axis 40 ms/div, 100 V/div) actual inductor current i_L (x-axis 40 ms/div, y-axis 10 A/div) and **(bottom)** its estimate $\hat{i}_L$ (x-axis 40 ms/div, y-axis 10 V/div) (only one phase).

6. CONCLUDING REMARKS

IN this thesis work an adaptive controller is proposed for a three-phase three-wire inverter, which compensates for unbalance and harmonic distortion. In other words, a controller was designed to allow the inverter to deliver an almost sinusoidal and balanced voltage, despite of a distorted and unbalanced load current. The controller is based on a weighted measurement of load and capacitor currents on the same current sensor, thus maintaining the number of sensors as in a conventional controller based on the capacitor current sensing. In the proposed arrangement of the current sensors a larger weight was associated to the capacitor currents, hence the obtained performance was very close to that of a controller based on capacitor current measurements, but with the advantage that information about the load current was also available. Therefore, it was possible to design a simple estimator for the inductor current, which was used for protection purposes. Another interesting observation was that, thanks to suitable transformations, the proposed controller was reduced to a controller with structure very close to the conventional one plus a bank of resonators, thus facilitating the implementation.

To experimentally prove the proposed controller and estimator, a three-phase three-wire UPS prototype was built. The power stage of the UPS system was based on a commercial three-phase VSI. An LC filter was connected at the output of the VSI to eliminate the switching effect of the devices. The unbalanced load was made with a three phase diode rectifier feeding a resistor, plus a resistor connected in between two phases to produce the unbalance condition. For the instrumentation of the inverter prototype, sensors, signal conditioners, voltage limiters and a control

interface have been implemented as well. The mixed current sensor was implemented with a CLN-50, which is a closed-loop hall effect current sensor. Another important observation was that all the control and measured signals were transmitted by means of shielded wire to reduce the noise. Different test have been carried out to assess the performance of the proposed controller and estimator. The tests include both steady state and transient responses. The experimental results with the proposed controller exhibit an improved performance in comparison with the conventional controller.

The controller presented here was obtained following adaptive techniques which gave, in principle, a stable and robust controller. However, in [30] it is demonstrated that, the sum (bank) of resonators has an alternative expression in terms of a single delay line. This expression can be easily built with a pure delay line in a negative feedback configuration plus a feedforward path. In fact, this new implementation belongs to the family of repetitive controllers. In other words, the whole bank of resonators can be replaced by the simpler repetitive scheme, thus, reducing the computational load, while preserving, and even improving, the performance. The resulting controller has a familiar and simple form which is suitable for implementation, where the most relevant feature is the introduction of the repetitive scheme. These results constitute the last additional work to this thesis that has not been included here because these results were obtained at the last minute. However, they have been presented recently in the international congress $PESC05$ [30].

An interesting task for the future consists also in improving the experimental settlement. First, the substitution of the dSPACE card by a reduced cost digital signal processor (DSP) card. Perhaps a fixed point DSP based card would be the most interesting from the cost point of view. Second, also the commercial VSI could be substituted by a VSI developed in the laboratory, and designed for the required power. Third, it would be preferable to have all signal conditioners and voltage limiters in the same card, placed close to the DSP control card. Notice that most of the sensors deliver currents as outputs, thus, a technique to alleviate the noise effects consists in transmitting such currents through the wires, and make the transformation to voltage only at the signal conditioners card where an instrumentation amplifier should be placed to reduce even more the effects of noise.

APPENDIX A. CLARKE'S TRANSFORMATION

The Clarke's transformation consists in a linear operator mapping from an orthogonal three-phase system to another, in other words, a space vector described in terms of 123-coordinates is described in another reference frame with only two orthogonal axis placed in the plane, and referred as $\alpha\beta$, and a third coordinate referred as γ or "0" component orthogonal to the plane. The 123-coordinates are also known in the literature as abc-coordinates or rts-coordinates. The main benefit of transforming to $\alpha\beta\gamma$-coordinates is that the γ coordinate is usually neglected, most of all in balanced three phase systems and in three-phase three-wire systems, thus reducing the model expressions and, most of all, the controller design work. A usual three-phase VSI is composed of three branches, also referred as legs, each formed with the cascade connection of two switching devices, as shown in Fig. 2.2. Both switching devices work in a complementary form, thus, the control of each branch is performed by a single control signal represented by u_i, $i \in \{1, 2, 3\}$, where every u_i takes values from the discrete set $\{0, 1\}$. The different combinations of such control signals can be represented as three dimensional space vectors described in 123-coordinates as can be seen in Fig. A.1(a).

The goal is to describe the vectors, relative to the original coordinate system 123, with respect to the orientation of the new rotated coordinate system $\alpha\beta\gamma$. This transformation is equivalent to perform two rotations given by the Euler's angles as described next. First, the 23-axes are rotated around the α-axis through an angle θ_1 counterclockwise. Second, the 12-axes are rotated around the β-axis through an angle θ_2 clockwise. These rotations are described by (A.1) and (A.2), respectively. They are shown in Fig. A.1(b), which describes how the rotated space $\alpha\beta\gamma$ shown in the Fig. A.1(c) is obtained.

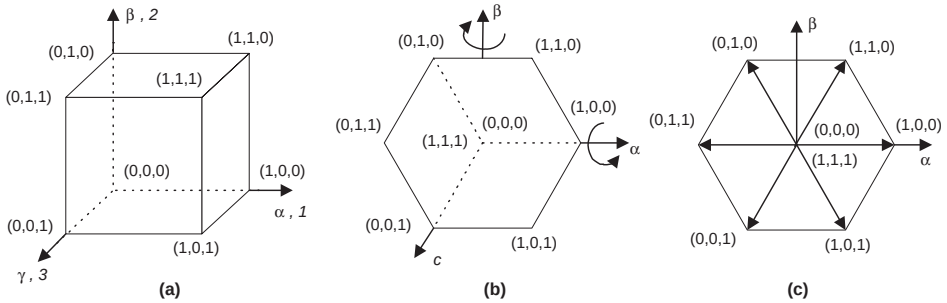

Fig. A.1: **(a)** Space vectors in 123-coordinates, **(b)** rotations to the transformed 123-coordinates into $\alpha\beta\gamma$-coordinates, and **(c)** resulting space vectors in $\alpha\beta\gamma$-coordinates.

$$R_\alpha(\theta_1) = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \cos(\theta_1) & -\sin(\theta_1) \\ 0 & \sin(\theta_1) & -\cos(\theta_1) \end{bmatrix} \tag{A.1}$$

$$R_\beta(\theta_2) = \begin{bmatrix} \cos(\theta_2) & 0 & -\sin(\theta_2) \\ 0 & 1 & 0 \\ \sin(\theta_2) & 0 & \cos(\theta_2) \end{bmatrix}. \tag{A.2}$$

The total rotation is described by the following matrix product

$$R(\theta_1, \theta_2) \;\; = \;\; R_\beta(\theta_2) R_\alpha(\theta_1). \tag{A.3}$$

After multiplication the following matrix is obtained

$$R(\theta_1, \theta_2) = \begin{bmatrix} \cos(\theta_2) & -\sin(\theta_1)\sin(\theta_2) & -\cos(\theta_1)\sin(\theta_2) \\ 0 & \cos(\theta_1) & -\sin(\theta_1) \\ \sin(\theta_2) & \sin(\theta_1)\cos(\theta_2) & \cos(\theta_1)\cos(\theta_2) \end{bmatrix}.$$

The previous matrix can be rewritten also as

$$R(\theta_1, \theta_2) = T = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{A.4}$$

where $\sin(\theta_1) = \cos(\theta_1) = \frac{1}{\sqrt{2}}$, $\sin(\theta_2) = \frac{1}{\sqrt{3}}$ and $\cos(\theta_2) = \sqrt{\frac{2}{3}}$ have been used. They represent the director cosines in terms of the Euler's angles. Moreover, the total rotation $R(\theta_1, \theta_2)$ has been concentrated in the matrix T, for which the following properties hold

$$\begin{aligned} T^{-1} &= T^T \\ T^{-1}T^T &= T^T T^{-1} = I \end{aligned}$$

where T^{-1} is the inverse matrix, T^T is the transposed matrix, and I is the unitary matrix. Therefore, the Clarke's transformation is defined as the transformation from space vectors in 123-coordinates to space vectors in $\alpha\beta\gamma$-coordinates and the opposite. It is applied in the following form.

$$\begin{aligned} x_{123} &= T x_{\alpha\beta\gamma} \\ x_{\alpha\beta\gamma} &= T^T x_{123} \end{aligned}$$

where $x_{123} = [x_1 \;\; x_2 \;\; x_3]^T$ and $x_{\alpha\beta\gamma} = [x_\alpha \;\; x_\beta, \; x_\gamma]^T$.

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